

COMPAL CONFIDENTIAL

MODEL NAME : JAZ00

PCB NO : LA-4291P

BOM P/N : 46155331L01



MINICOOPER

**uFCBGA Mobile Penryn SFF ULV
Intel Cantiga GS(High Performance) + ICH9M SFF**

12-07-2007
REV : 0.1(X00)
www.altech1.ru

@ : Nopop Component

1@ : TAA board Used only

2@ : Without TAA board Used only

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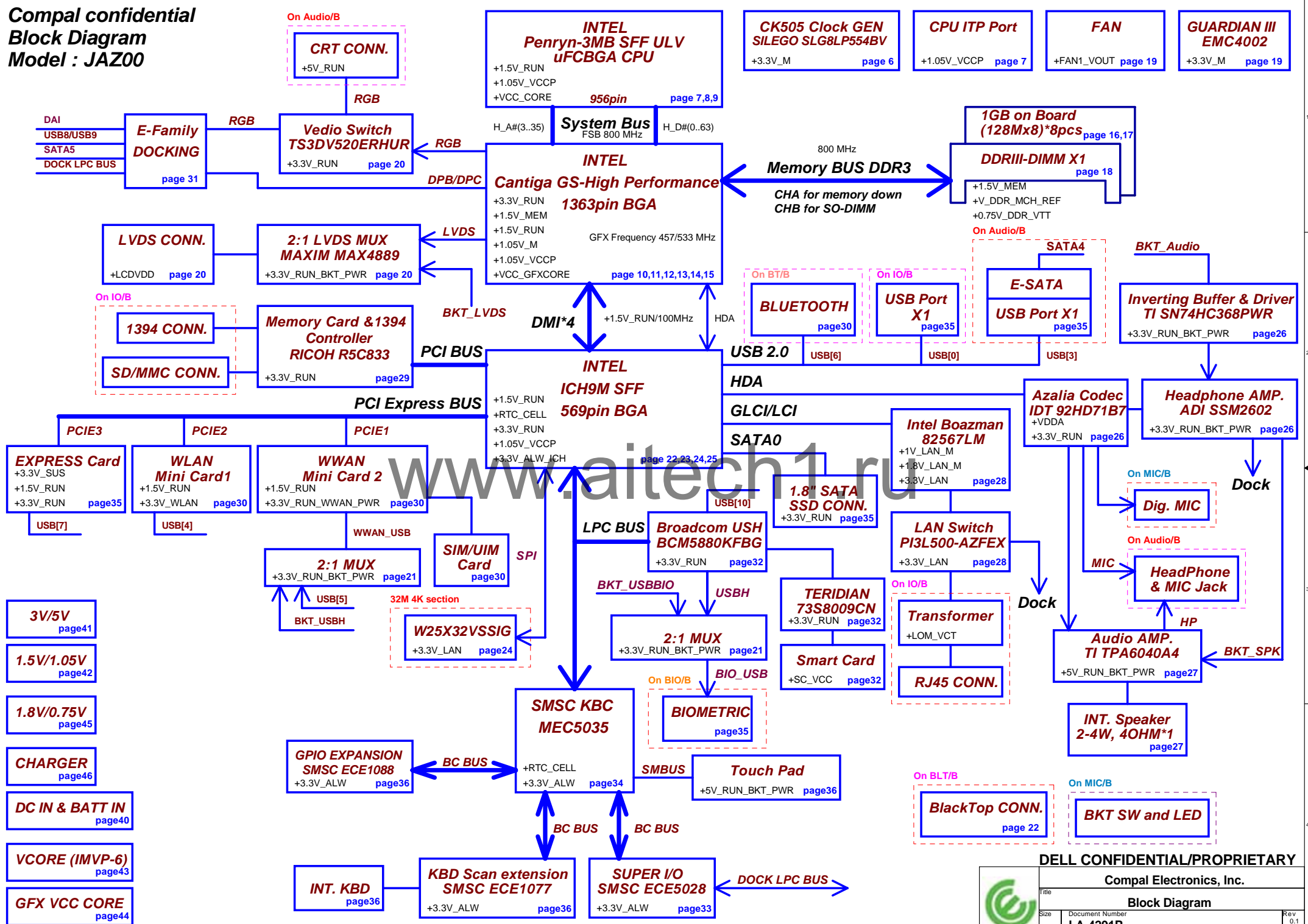
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Title			
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Block Diagram
Model : JAZ00



POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

USB PORT#	DESTINATION
0	JUSB (Ext Right Side)
1	NONE
2	NONE
3	JESATA (Ext Left Side)
4	WLAN
5	WWAN
6	BT
7	Express card
8	DOCKING
9	DOCKING
10	USH->BIO
11	NONE

PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW +3.3V_ALW_ICH +3.3V_RTC_LDO +1.5V_ALW_HDA	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_GFXCORE +VCC_CORE +1.05V_VCCP	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)	+3.3V_RUN_BKT_PWR +5V_RUN_BKT_PWR +3.3V_RUN_WWAN_PWR +INV_PWR_SRC +LCDVDD	+3.3V_BKT_PWR
S0	ON	ON	ON	ON	ON	ON	OFF
S3	ON	ON	OFF	ON	OFF	OFF	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF	OFF	OFF
BLT mode	ON	OFF	OFF	OFF	OFF	ON	ON

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-2 WWAN
Lane 2	MINI CARD-1 WLAN
Lane 3	None
Lane 4	EXPRESS CARD
Lane 5	None
Lane 6	Giga LAN

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	AD17	REQ#1 / GNT#1	PIRQ[C..D]

SATA	DESTINATION
SATA0	SSD
SATA1	None
SATA4	ESATA
SATA5	DOCKING

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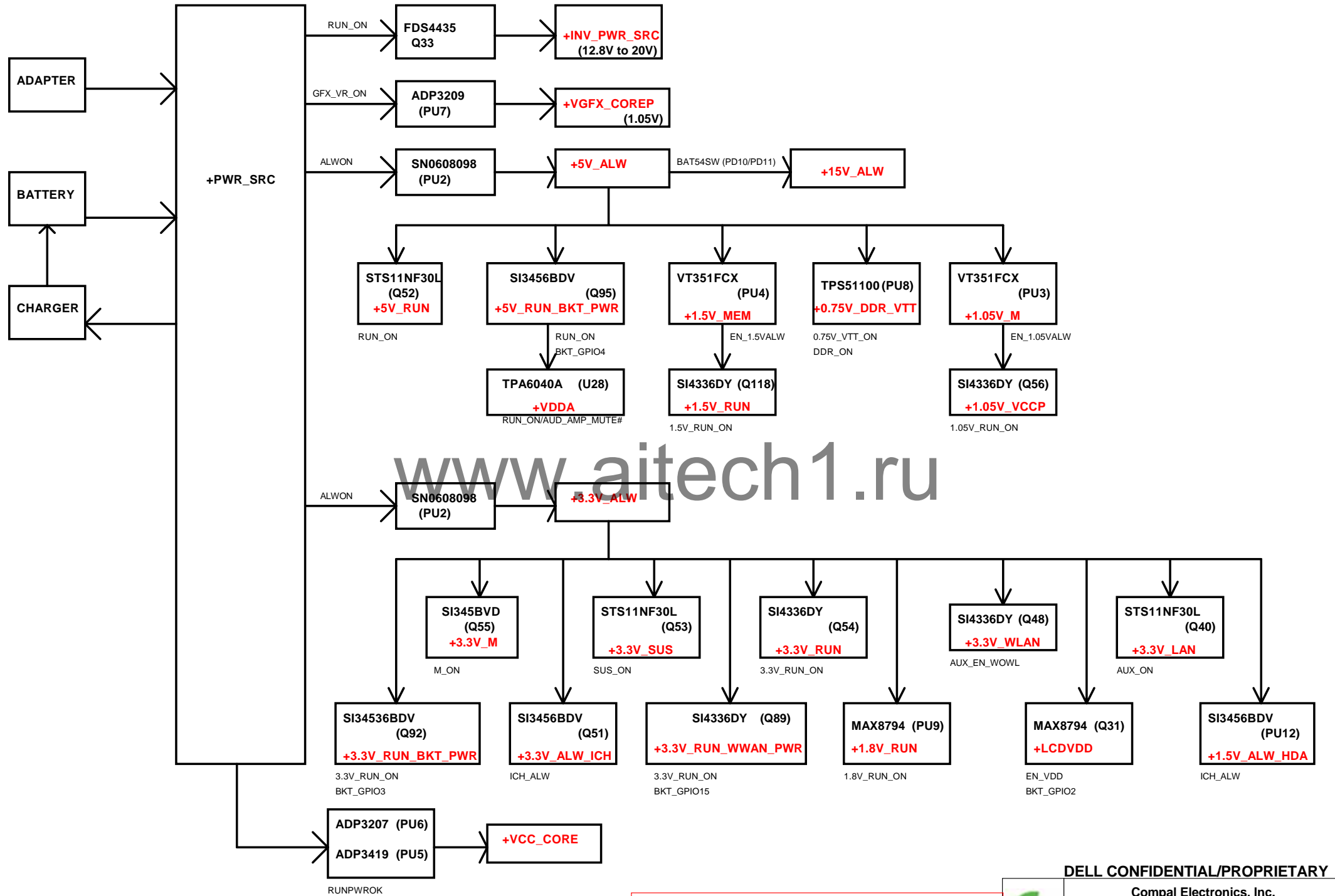
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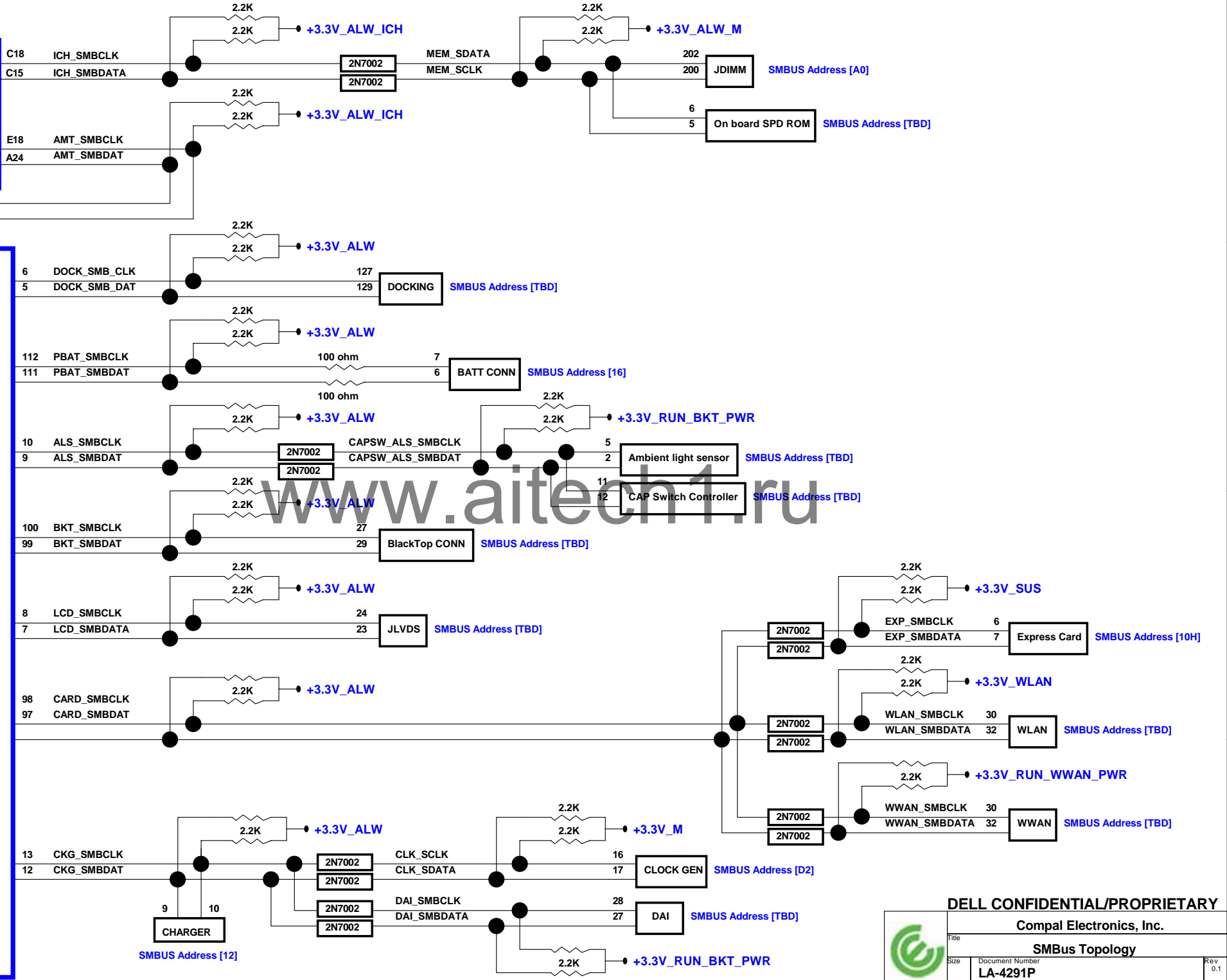
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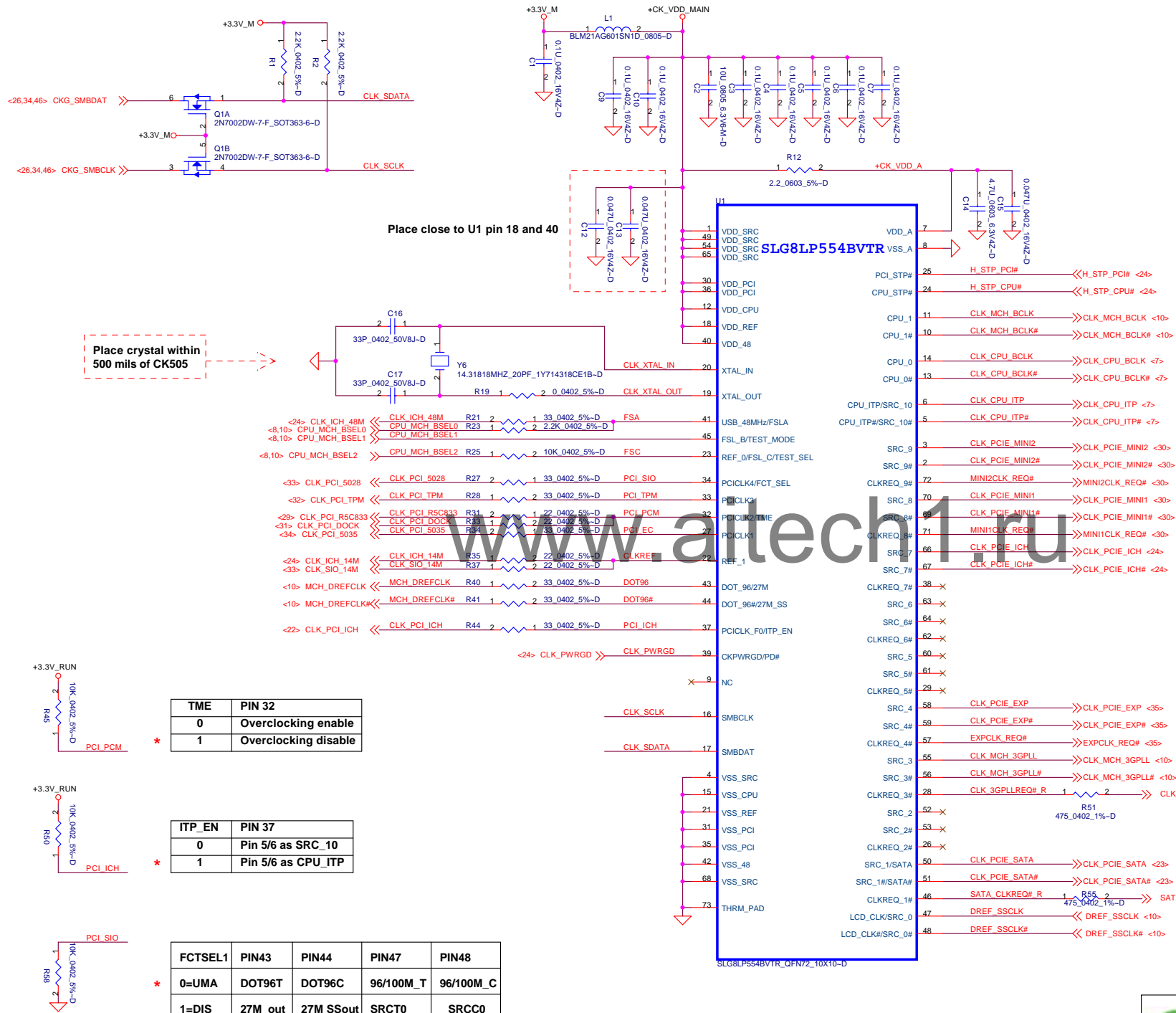




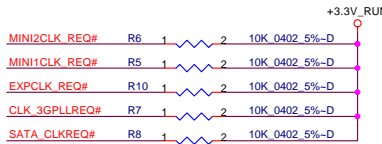
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FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3



TME	PIN 32
0	Overclocking enable
1	Overclocking disable

ITP_EN	PIN 37
0	Pin 5/6 as SRC_10
1	Pin 5/6 as CPU_ITP

FCTSEL1	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1=DIS	27M_out	27M SSout	SRCT0	SRCC0

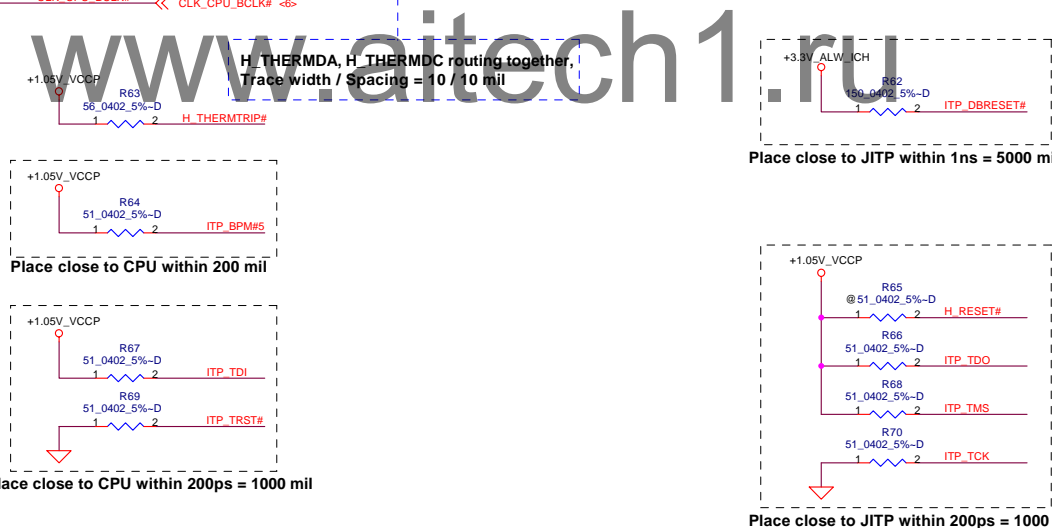
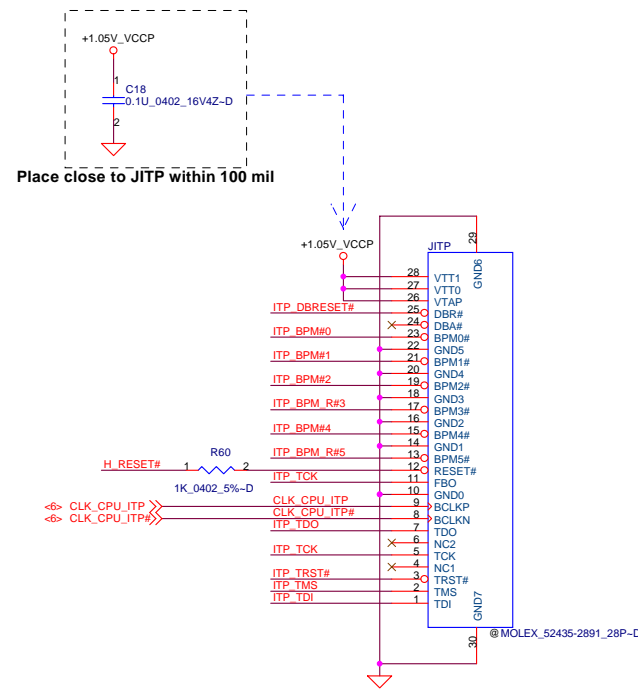
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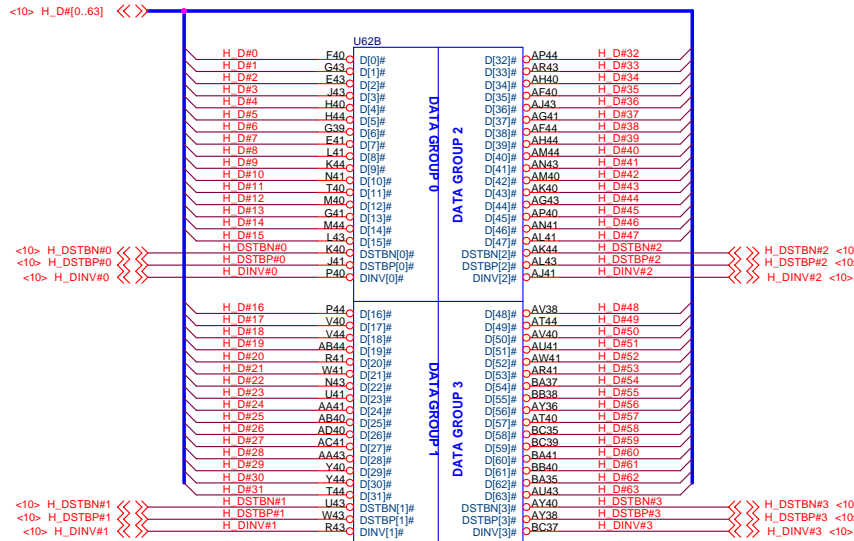


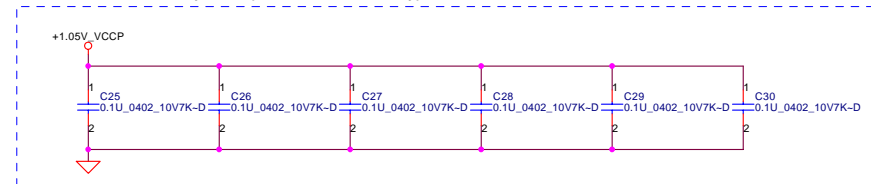
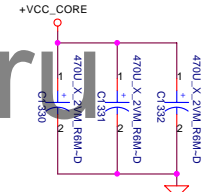
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D

C

B

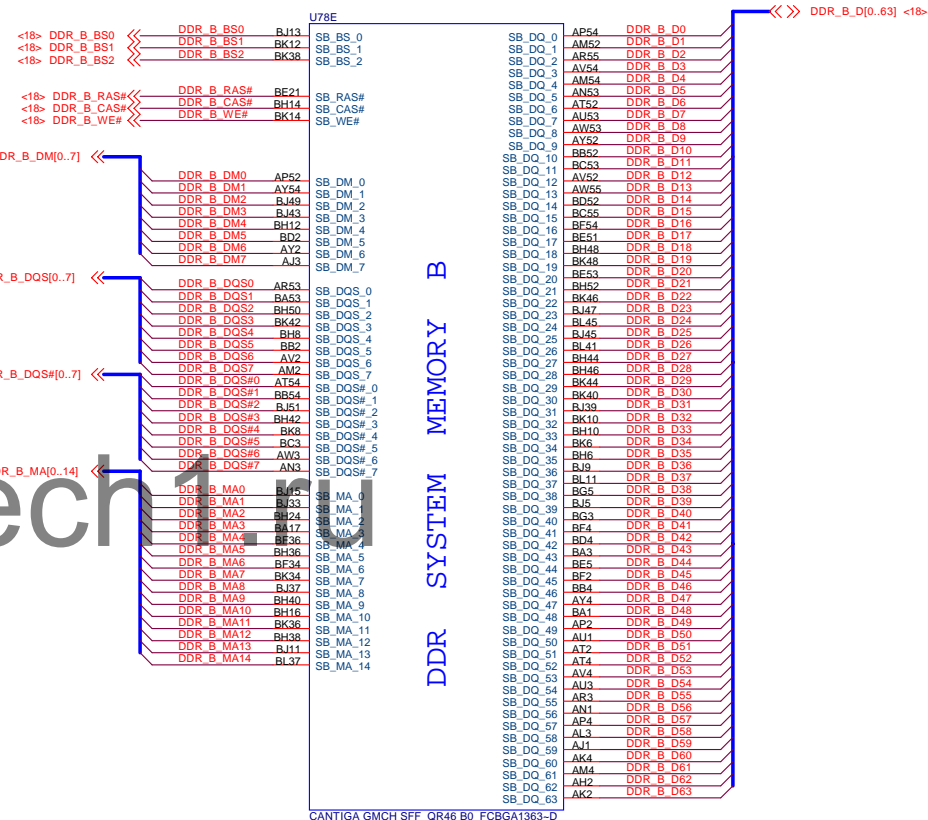
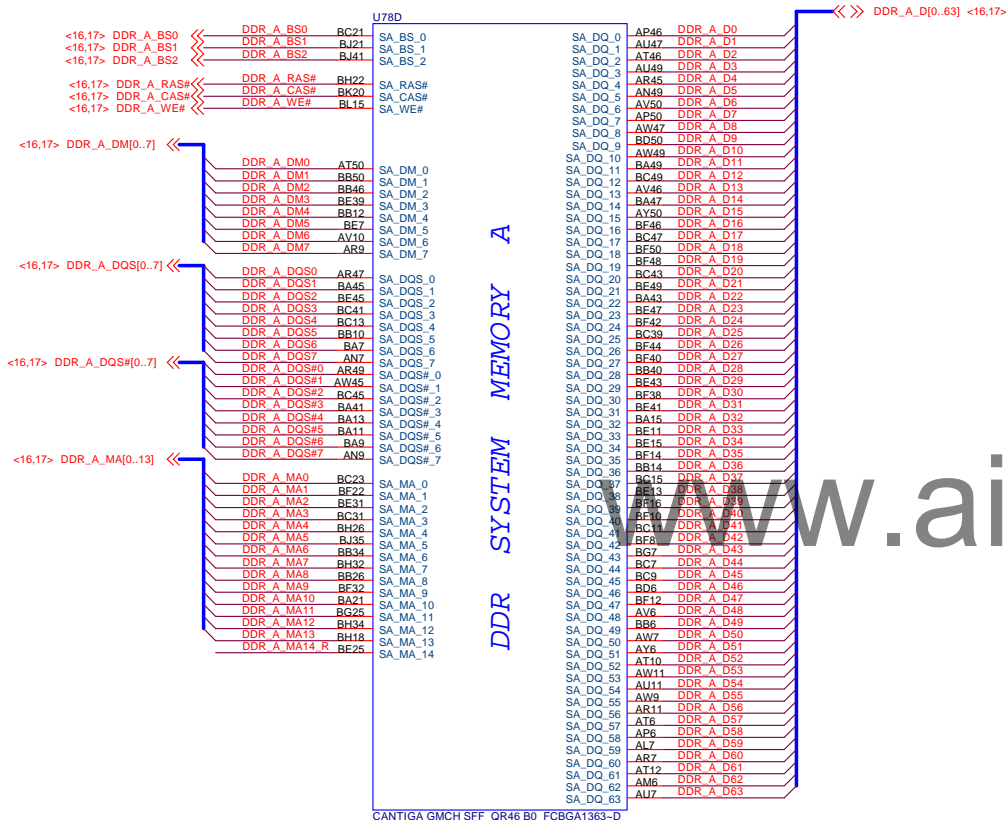
A

D

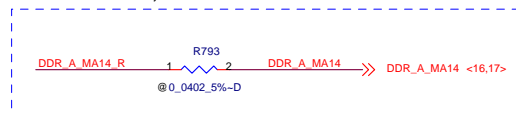
C

B

A



Place close to U78, reserve for 2Gb on board RAMs



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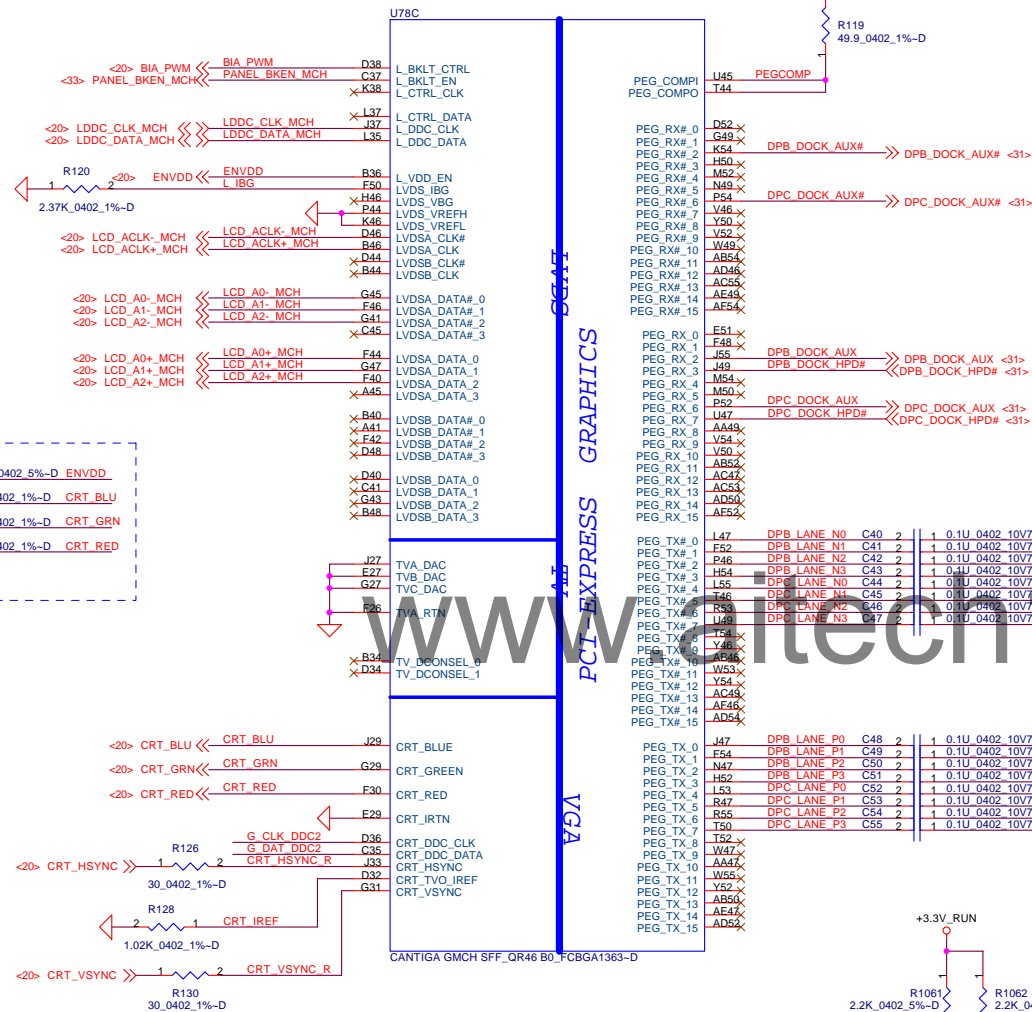


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Cantiga GS(2/6)

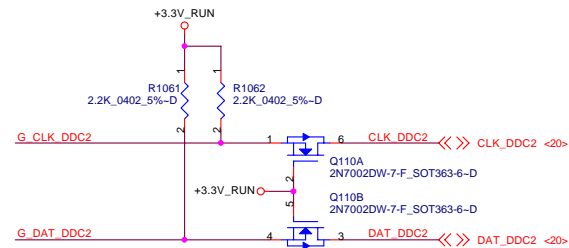
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Strap Pin Table		
CFG5	DMI X2 Select	Low = DMI x 2 High = DMI x 4 (Default)
CFG6	iTPM Host Interface	Low = iTPM enable High = iTPM disable(Default)
CFG7	Management Engine Crypto Strap	Low = TLS cipher suite with no confidentiality High = TLS cipher suite with confidentiality(Default)
CFG9	PCI Express Graphic Lane	Low = Reverse Lane High = Normal Operation(Default)
CFG10	PCI Express Lookpack enable	Low = Enable High = Disable(default)
CFG12	ALLZ	Low = ALLZ mode enable High = Disable(default)
CFG13	XOR	Low = XOR mode enable High = Disable(default)
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default)
CFG19	DMI Lane Reversal	Low=Normal (default) High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIe1 is operational (default) High=SDVO and PCIe1 are operating simultaneously via PEG port
SDVO_CTRL_DATA		Low=No SDVO Device Present (default) High=SDVO Device Present
DDPC_CTRL_DATA		Low=DisplayPort disabled (default) High=DisplayPort device present

CFG[5:16] have internal pullup

CFG[19:20] have internal pulldown



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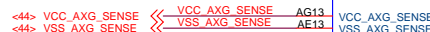
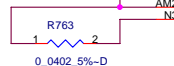
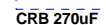
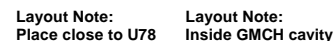


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BA55	VSS_1	VSS_100	C43
AU55	VSS_2	VSS_101	A43
AN55	VSS_3	VSS_102	BD42
AJ55	VSS_4	VSS_103	H42
AE55	VSS_5	VSS_104	BQ41
AA55	VSS_6	VSS_105	AY41
U55	VSS_7	VSS_106	AU41
N55	VSS_8	VSS_107	AM41
BD54	VSS_9	VSS_108	AU41
BG53	VSS_10	VSS_109	AG41
AJ53	VSS_11	VSS_110	AE41
AE53	VSS_12	VSS_111	AA41
AA53	VSS_13	VSS_112	R41
U53	VSS_14	VSS_113	M41
N53	VSS_15	VSS_114	E41
J53	VSS_16	VSS_115	BD40
GS5	VSS_17	VSS_116	AU40
E53	VSS_18	VSS_117	AR40
K52	VSS_19	VSS_118	AN40
BG51	VSS_20	VSS_119	W40
BA51	VSS_21	VSS_120	U40
AW51	VSS_22	VSS_121	T40
AU51	VSS_23	VSS_122	R40
AR51	VSS_24	VSS_123	K40
AN51	VSS_25	VSS_124	H40
AL51	VSS_26	VSS_125	BL39
AJ51	VSS_27	VSS_126	BG39
AG51	VSS_28	VSS_127	BA39
AE51	VSS_29	VSS_128	E39
AC51	VSS_30	VSS_129	C39
AA51	VSS_31	VSS_130	A39
W51	VSS_32	VSS_131	BD38
U51	VSS_33	VSS_132	AU38
R51	VSS_34	VSS_133	H38
N51	VSS_35	VSS_134	BG37
L51	VSS_36	VSS_135	AU37
J51	VSS_37	VSS_136	M37
GS1	VSS_38	VSS_137	BD36
BK50	VSS_39	VSS_138	E37
BG49	VSS_40	VSS_139	AW36
AM50	VSS_41	VSS_140	H36
K50	VSS_42	VSS_141	BL35
E49	VSS_43	VSS_142	BG35
C49	VSS_44	VSS_143	AY35
BD48	VSS_45	VSS_144	AU35
BG48	VSS_46	VSS_145	AL35
AY48	VSS_47	VSS_146	AG35
AV48	VSS_48	VSS_147	AE35
AT48	VSS_49	VSS_148	AA35
AP48	VSS_50	VSS_149	Y35
AM48	VSS_51	VSS_150	M35
AK48	VSS_52	VSS_151	E35
AH48	VSS_53	VSS_152	A35
AD48	VSS_54	VSS_153	BD34
AB48	VSS_55	VSS_154	AU34
Y48	VSS_56	VSS_155	AN34
T48	VSS_57	VSS_156	H34
P48	VSS_58	VSS_157	BL33
M48	VSS_59	VSS_158	BG33
K48	VSS_60	VSS_159	E33
H48	VSS_61	VSS_160	LE33
BL47	VSS_62	VSS_161	BD32
BG47	VSS_63	VSS_162	AU32
E47	VSS_64	VSS_163	AN32
C47	VSS_65	VSS_164	AG32
A47	VSS_66	VSS_165	AC32
BD46	VSS_67	VSS_166	Y32
AY46	VSS_68	VSS_167	H32
AM46	VSS_69	VSS_168	B32
AK46	VSS_70	VSS_169	BL31
AH46	VSS_71	VSS_170	BG31
AD46	VSS_72	VSS_171	AY31
AB46	VSS_73	VSS_172	AN31
Y46	VSS_74	VSS_173	M31
T46	VSS_75	VSS_174	E31
P46	VSS_76	VSS_175	N30
M46	VSS_77	VSS_176	H30
K46	VSS_78	VSS_177	AN29
H46	VSS_79	VSS_178	AJ29
BL43	VSS_80	VSS_179	M29
BG43	VSS_81	VSS_180	A29
E43	VSS_82	VSS_181	AW28
C43	VSS_83	VSS_182	AN28
BD44	VSS_84	VSS_183	H28
AY44	VSS_85	VSS_184	AD28
AM44	VSS_86	VSS_185	AC28
AK44	VSS_87	VSS_186	Y28
AH44	VSS_88	VSS_187	W28
AD44	VSS_89	VSS_188	H28
AB44	VSS_90	VSS_189	F28
Y44	VSS_91	VSS_190	AN27
T44	VSS_92	VSS_191	AJ27
P44	VSS_93	VSS_192	M27
M44	VSS_94	VSS_193	BD26
K44	VSS_95	VSS_194	N26
H44	VSS_96	VSS_195	H26
BL43	VSS_97	VSS_196	BL25
BG43	VSS_98	VSS_197	AY25
E43	VSS_99	VSS_198	AU25

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U78J

AN25	VSS_199	VSS_300	AM8
AG25	VSS_200	VSS_301	AK8
AE25	VSS_201	VSS_302	AH8
AA25	VSS_202	VSS_303	AF8
Y25	VSS_203	VSS_304	AD8
E25	VSS_204	VSS_305	AB8
A25	VSS_205	VSS_306	Y8
BD24	VSS_206	VSS_307	V8
AN24	VSS_207	VSS_308	P8
AL24	VSS_208	VSS_309	M8
H24	VSS_209	VSS_310	K8
BG23	VSS_210	VSS_311	H8
E23	VSS_211	VSS_312	B17
BD22	VSS_212	VSS_313	E7
BB22	VSS_213	VSS_314	BF6
AN22	VSS_214	VSS_315	BC5
Y22	VSS_215	VSS_316	BA5
W22	VSS_216	VSS_317	AW5
H22	VSS_217	VSS_318	AU5
BL21	VSS_218	VSS_319	AR5
BG21	VSS_219	VSS_320	AN5
AY21	VSS_220	VSS_321	AL5
AN21	VSS_221	VSS_322	AJ5
AG21	VSS_222	VSS_323	AG5
AE21	VSS_223	VSS_324	AE5
E21	VSS_224	VSS_325	AC5
A21	VSS_225	VSS_326	AA5
BD20	VSS_226	VSS_327	W5
H20	VSS_227	VSS_328	U5
BG19	VSS_228	VSS_329	N5
AY19	VSS_229	VSS_330	L5
E19	VSS_230	VSS_331	J5
BD18	VSS_231	VSS_332	G5
N18	VSS_232	VSS_333	C5
E18	VSS_233	VSS_334	BH4
BD17	VSS_234	VSS_335	BE3
BL17	VSS_235	VSS_336	U3
BG17	VSS_236	VSS_337	E3
AY17	VSS_237	VSS_338	BC1
M17	VSS_238	VSS_339	AW1
E17	VSS_239	VSS_340	AR1
A17	VSS_240	VSS_341	AL1
BD16	VSS_241	VSS_342	AG1
AN16	VSS_242	VSS_343	AC1
AG16	VSS_243	VSS_344	W1
AE16	VSS_244	VSS_345	N1
Y16	VSS_245	VSS_346	J1
W16	VSS_246	VSS_347	AU43
M16	VSS_247	VSS_348	BB42
H16	VSS_248	VSS_349	AW38
BG15	VSS_249	VSS_350	BA35
AY15	VSS_250	VSS_351	L29
AN15	VSS_251	VSS_352	N28
AG15	VSS_252	VSS_353	N22
AE15	VSS_253	VSS_354	N20
Y15	VSS_254	VSS_355	N14
BD14	VSS_255	VSS_356	AL13
BL14	VSS_256	VSS_357	B10
BG13	VSS_257	VSS_358	AN13
AY13	VSS_258	VSS_359	N42
AN13	VSS_259	VSS_360	N40
AG13	VSS_260	VSS_361	N38
AE13	VSS_261	VSS_362	M39
Y13	VSS_262		
W13	VSS_263		
BD12	VSS_264		
AN12	VSS_265		
AG12	VSS_266		
AE12	VSS_267		
Y12	VSS_268		
W12	VSS_269		
M12	VSS_270		
E12	VSS_271		
BD11	VSS_272		
AN11	VSS_273		
AG11	VSS_274		
AE11	VSS_275		
Y11	VSS_276		
BD10	VSS_277		
BL10	VSS_278		
BG10	VSS_279		
AY10	VSS_280		
AN10	VSS_281		
AG10	VSS_282		
AE10	VSS_283		
Y10	VSS_284		
W10	VSS_285		
M10	VSS_286		
B10	VSS_287		
AN10	VSS_288		
H10	VSS_289		
BL9	VSS_290		
BG9	VSS_291		
E9	VSS_292		
A9	VSS_293		
BD8	VSS_294		
B8	VSS_295		
AY8	VSS_296		
AV8	VSS_297		
AT8	VSS_298		
AP8	VSS_299		

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VSS

VSS

VSS NCTF

VSS SCB

VSS NCTF_1
VSS NCTF_2
VSS NCTF_3
VSS NCTF_4
VSS NCTF_5
VSS NCTF_6
VSS NCTF_7
VSS NCTF_8
VSS NCTF_9
VSS NCTF_10
VSS NCTF_11
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VSS SCB_3
VSS SCB_4
VSS SCB_5
VSS SCB_6
VSS SCB_7A138
AH38
AD38
AC38
T35
R35
AT32
AR32
U32
R32
T28
AT25
AR25
T24
R24
AN19
AJ19
AA19
Y19
T19
R19
AN18BL55
BL1
AS5
D1
B55
B2
A4

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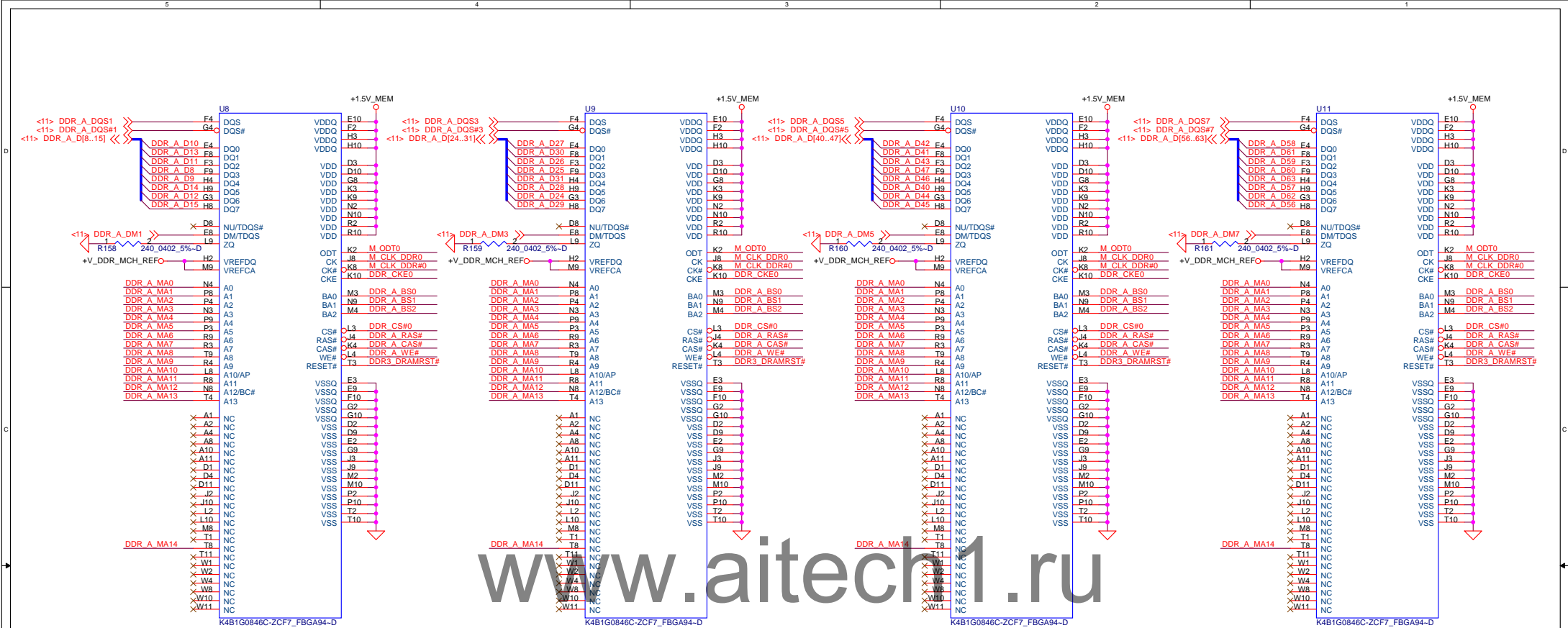
Compal Electronics, Inc.

Cantiga GS(6/6)

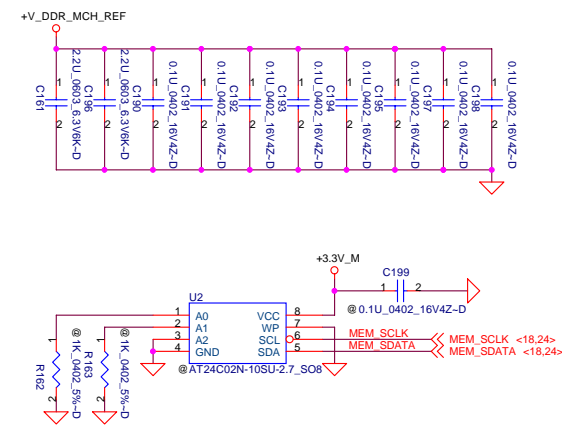


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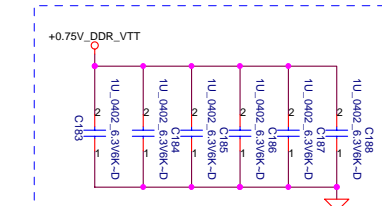
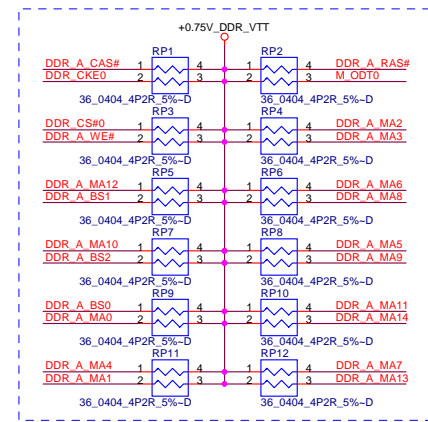
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- <11,16> DDR_A_MA[0..14] <<>
- <10,16> M_ODT0 <> M_ODT0
- <10,16> M_CLK_DDR0 <> M_CLK_DDR0
- <10,16> M_CLK_DDR#0 <> M_CLK_DDR#0
- <10,16> DDR_CKE0 <> DDR_CKE0
- <11,16> DDR_A_BS0 <> DDR_A_BS0
- <11,16> DDR_A_BS1 <> DDR_A_BS1
- <11,16> DDR_A_BS2 <> DDR_A_BS2
- <10,16> DDR_CS#0 <> DDR_CS#0
- <11,16> DDR_RAS# <> DDR_A_RAS#
- <11,16> DDR_CAS# <> DDR_A_CAS#
- <11,16> DDR_A_WE# <> DDR_A_WE#
- <10,16,18> DDR3_DRAMRST# <> DDR3_DRAMRST#



DDR3 Terminations



Place decaps close end termination resistors, one decap for 4 resistors

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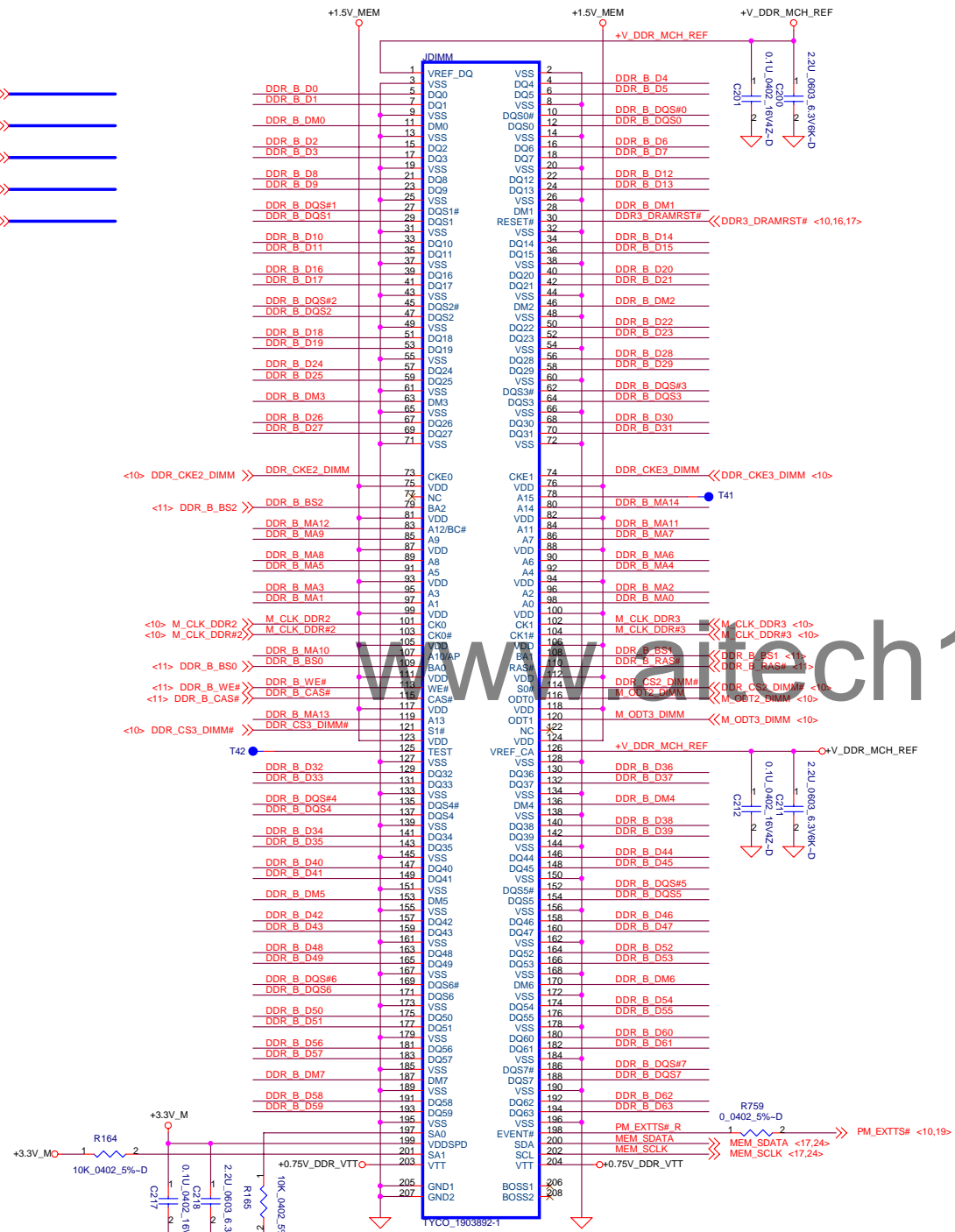
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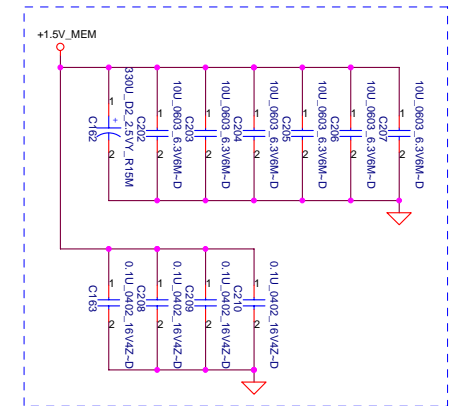
DDR3II-Memory Down (Bottom)

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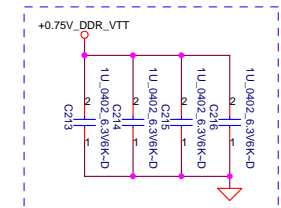
<11> DDR_B_D[0..63] <<>>
<11> DDR_B_DQS[0..7] <<>>
<11> DDR_B_DM[0..7] <<>>
<11> DDR_B_MA[0..14] <<>>



Place close to SO-DIMM



Place close to JDIMM pin 203 and 204



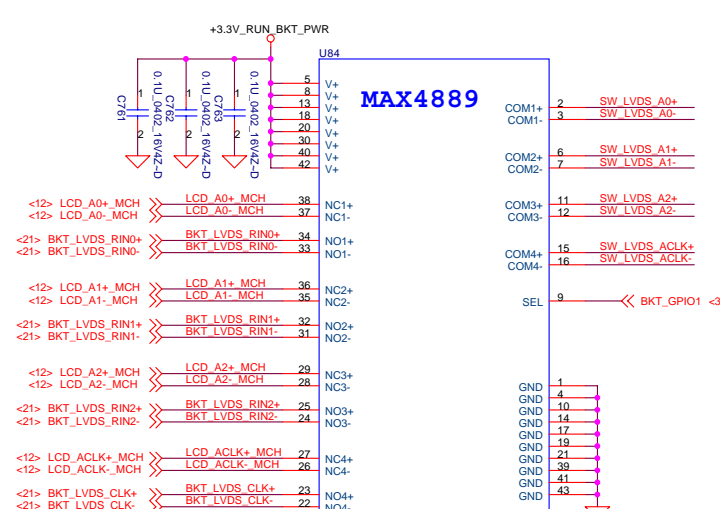
DDR3 SO-DIMM/Standard Type

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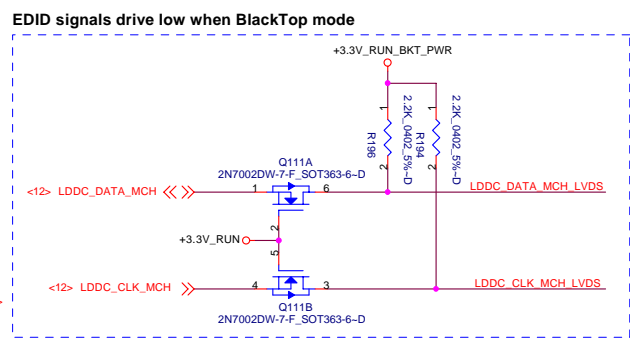


Compal Electronics, Inc.		
DDR3 SO-DIMM SLOT		
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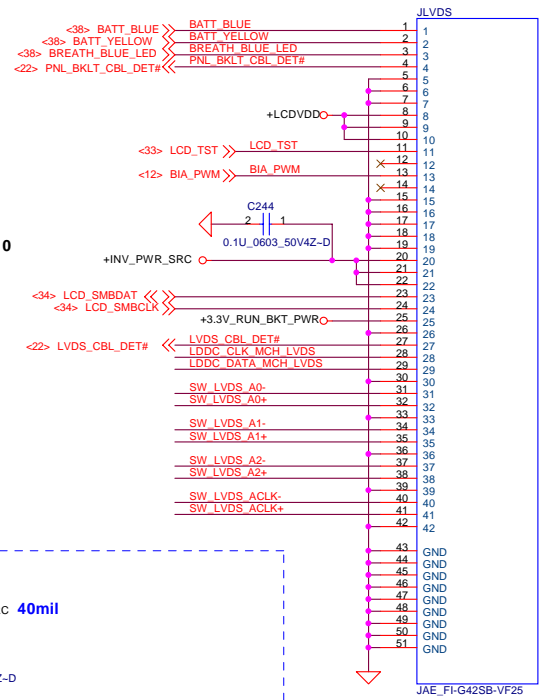
SEL Logic 1 Work from BKT

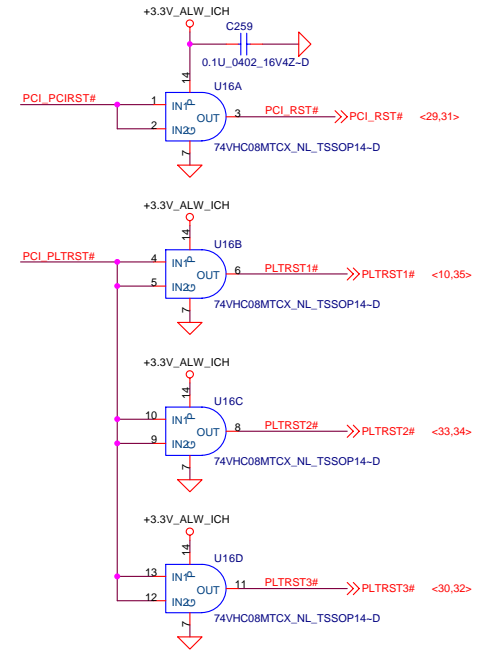
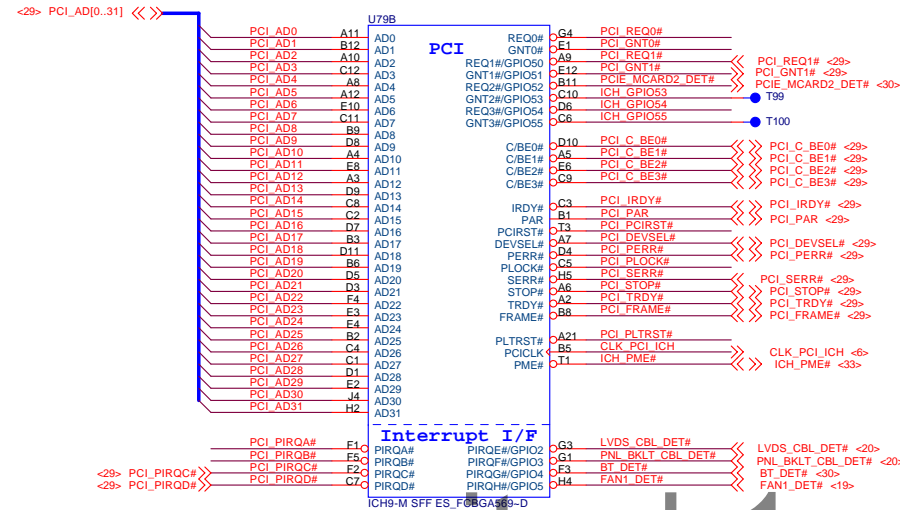
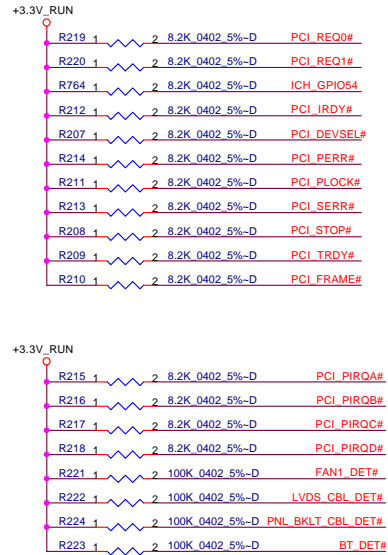
SEL	NC to COM	NO to COM
0	ON	OFF
1	OFF	ON



Place close to JLVDS.8,9,10

Place close to JLVDS.25

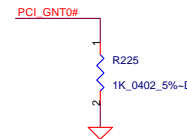




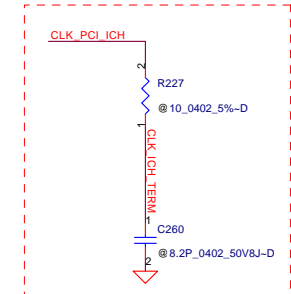
There is a weak integrated pull-up resistor on SPI_CS#1 pin

Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Destination
0	1	SPI
1	0	PCI
1	1	LPC

*



Place closely pin U79.B5

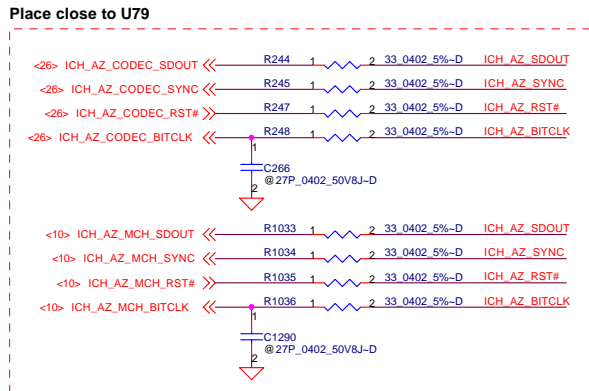


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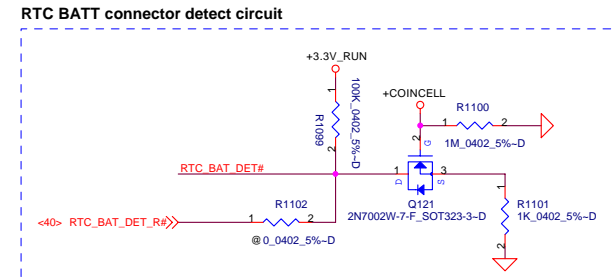
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Title		ICH9M SFF(1/4)	
Size	Document Number	Rev	
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ME_CLR	TPM setting
Short	Clear ME RTC Registers
Open	Keep ME RTC Registers

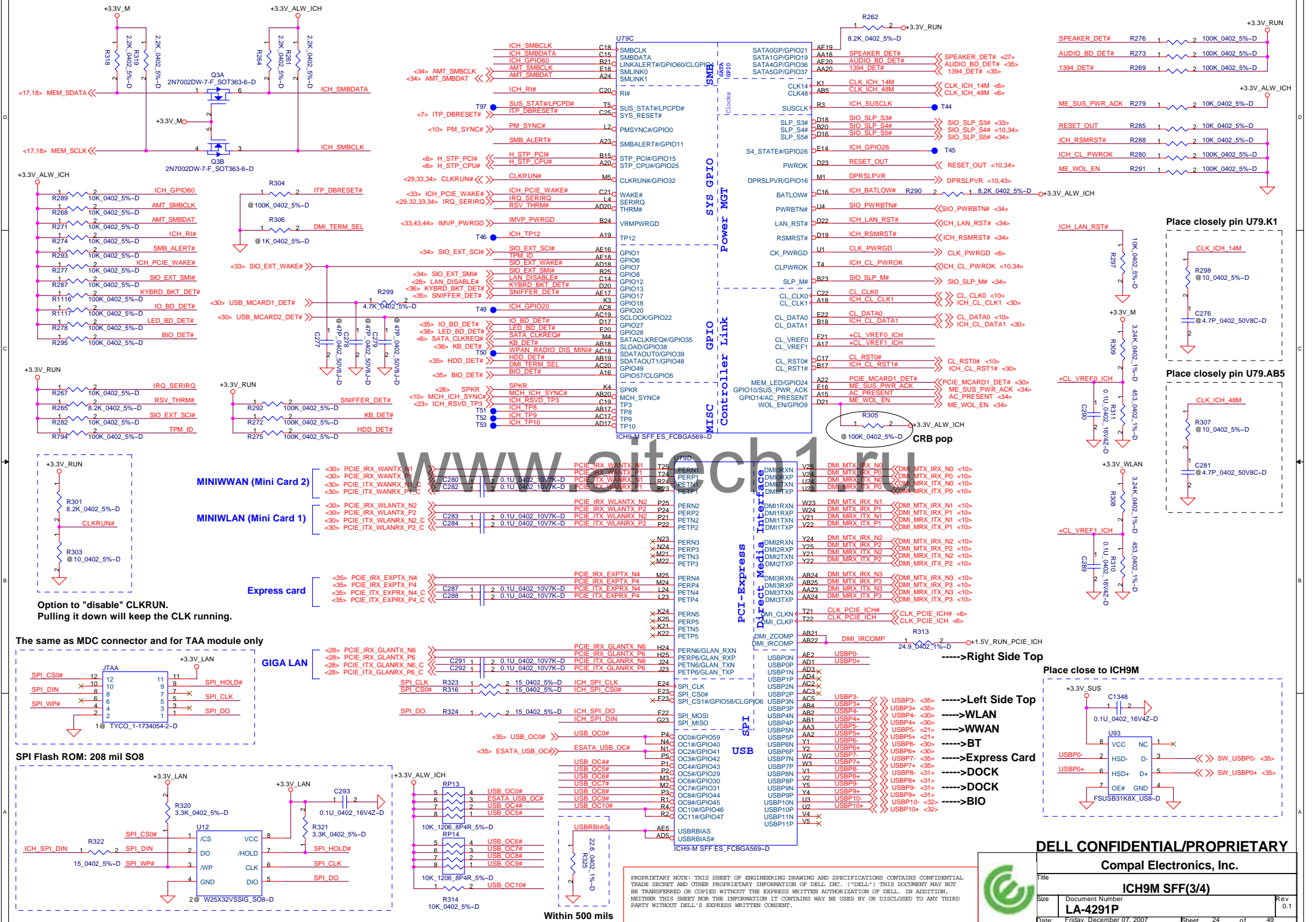


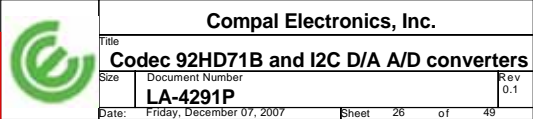
There is a weak integrated pull-up resistor on ICH_RSVD_TP3 pin
There is a weak integrated pull-down resistor on HDA_SDOUT pin

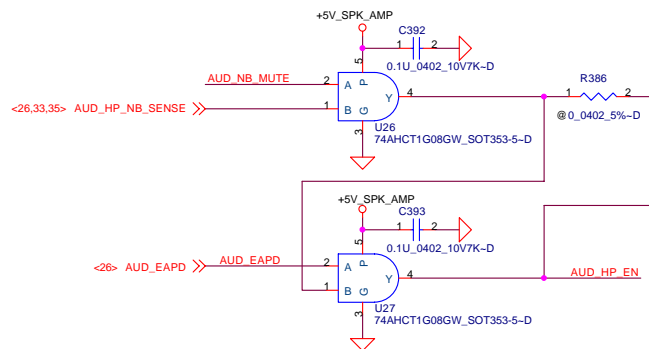


	Compal Electronics, Inc.			
	Title			
	ICH9M SFF(2/4)			
	Size	Document Number	Rev	
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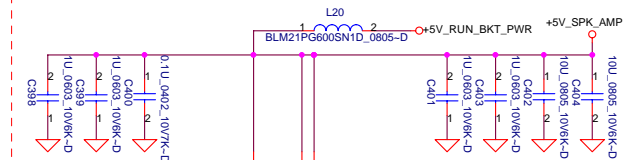




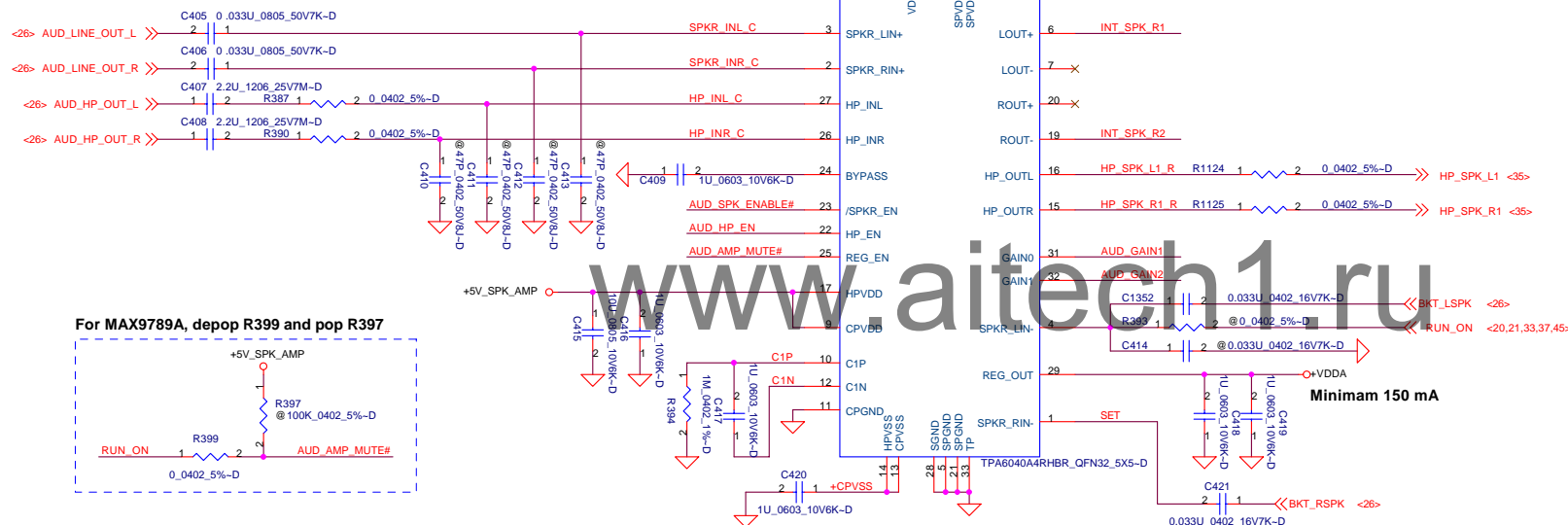
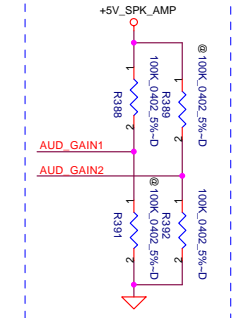


Place close to Audio Chip

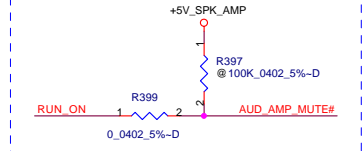
W=40mils



Gain Setting for TPA6040A4

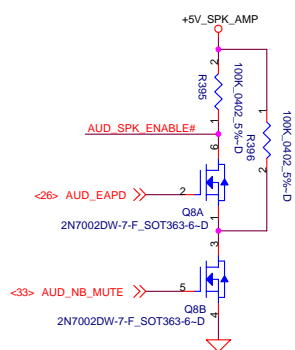
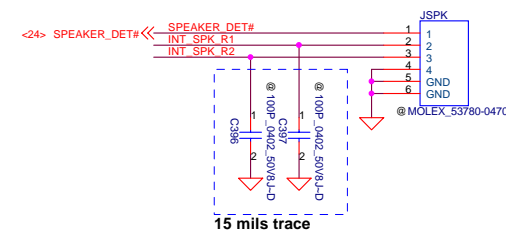


For MAX9789A, depop R399 and pop R397



GAIN1	GAIN2	AV(inv)	INPUT IMPEDANCE
0	0	6dB	82K ohm
0	1	10dB	66K ohm
1	0	15.6dB	45K ohm
1	1	21.6dB	26K ohm

Minimam 150 mA



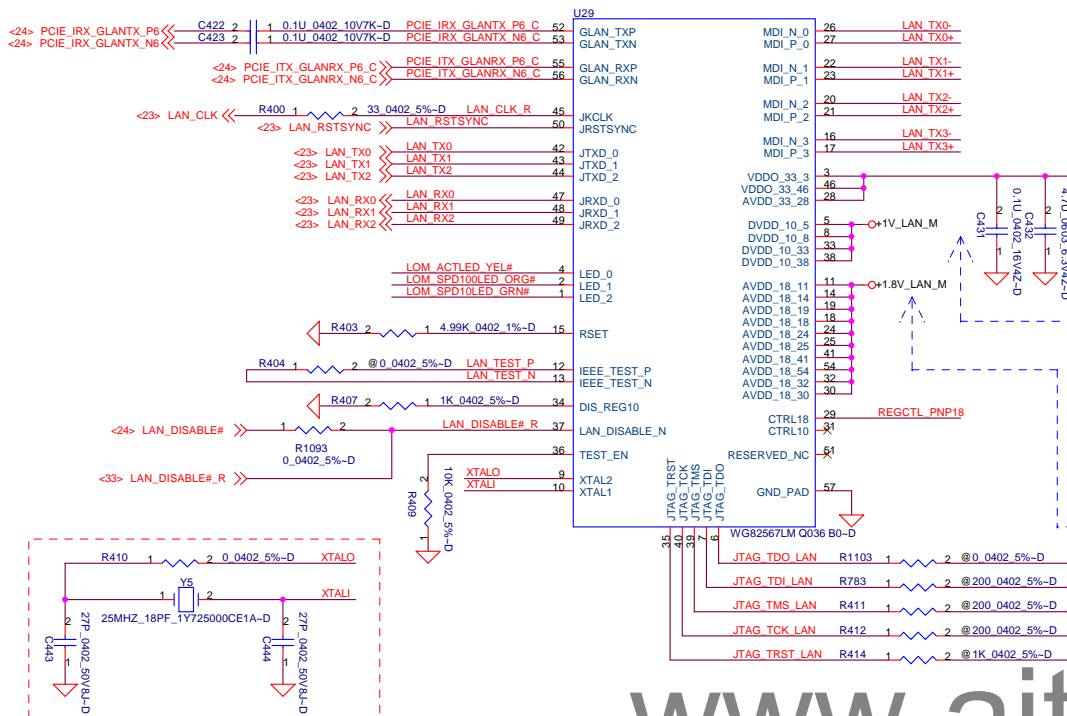
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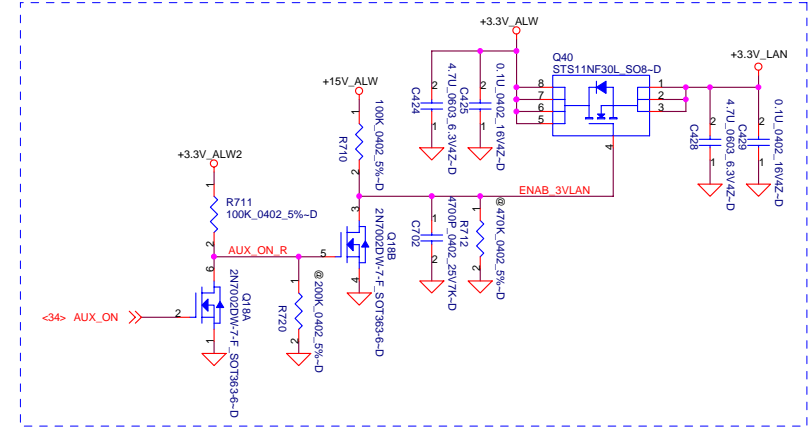
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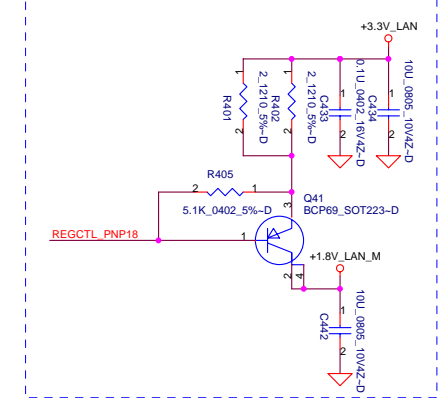
Title		Audio amplifier and speaker CONN	
Size	Document Number	Rev	0.1
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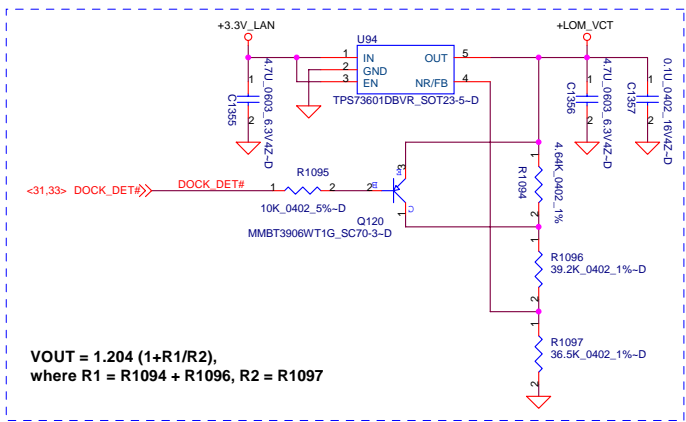
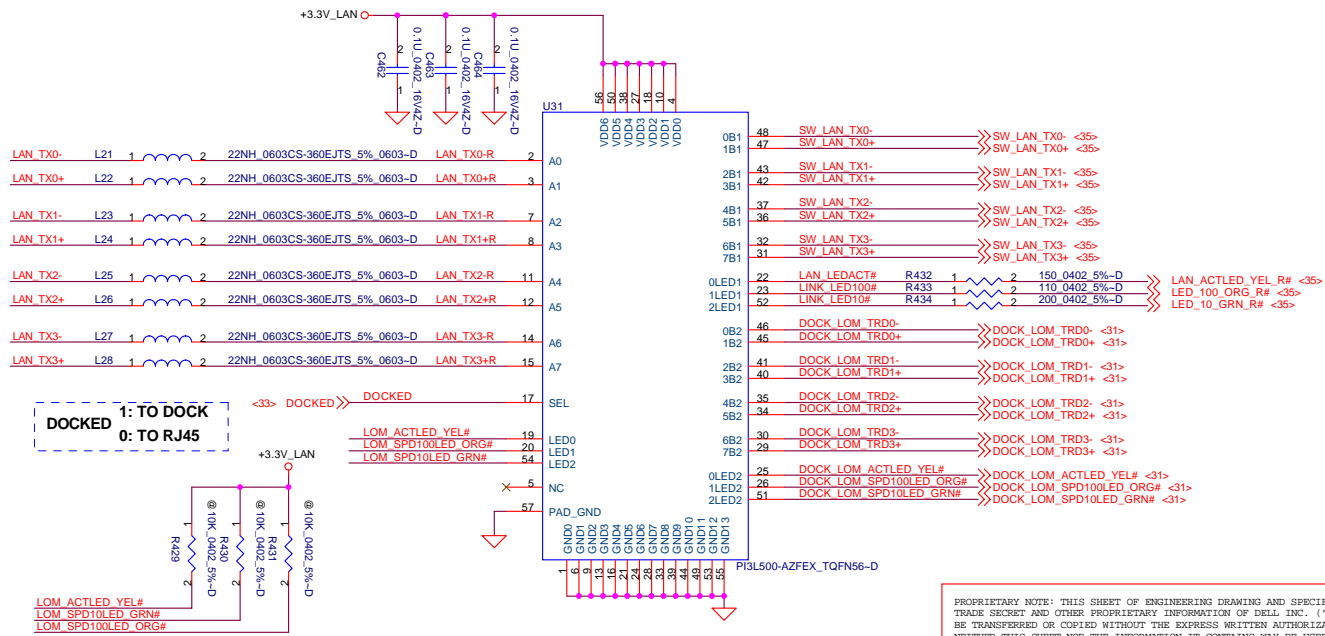
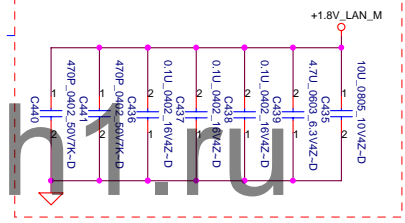
+3.3V_LAN SOURCE



+1.8V_LAN_M regulator control



Place close to U29



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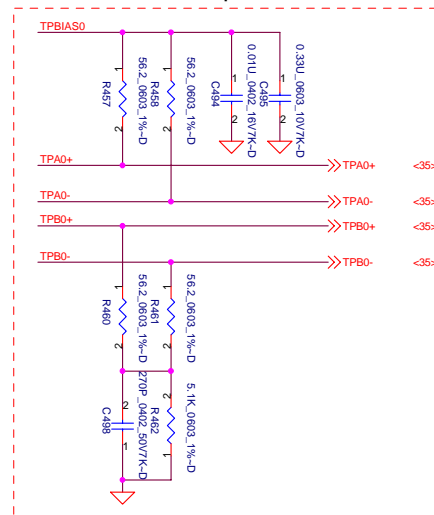


Boazman 82567LM and LAN SWITCH	
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UDIO3	UDIO4	MSEN	XDEN	Function
Pull-up	Pull-up	Pull-down	Pull-down	Enable SD,MMC Card

Media I/F	SD Card	MMC Card
MDIO00	SDCD#	MMCCD#
MDIO01		
MDIO02		
MDIO03	SDWP#	
MDIO04	SDPWR0	MMCPWR
MDIO05	SDPWR1	
MDIO06	SDLED#	MMCLEd#
MDIO07	SDEXTCK	
MDIO08	SDCCMD	MMCCMD
MDIO09	SDCCLK	MMCCLK
MDIO10	SDCDAT0	MMCDAT0
MDIO11	SDCDAT1	MMCDAT1
MDIO12	SDCDAT2	MMCDAT2
MDIO13	SDCDAT3	MMCDAT3
MDIO14		MMCDAT4
MDIO15		MMCDAT5
MDIO16		MMCDAT6
MDIO17		MMCDAT7
MDIO18		
MDIO19		



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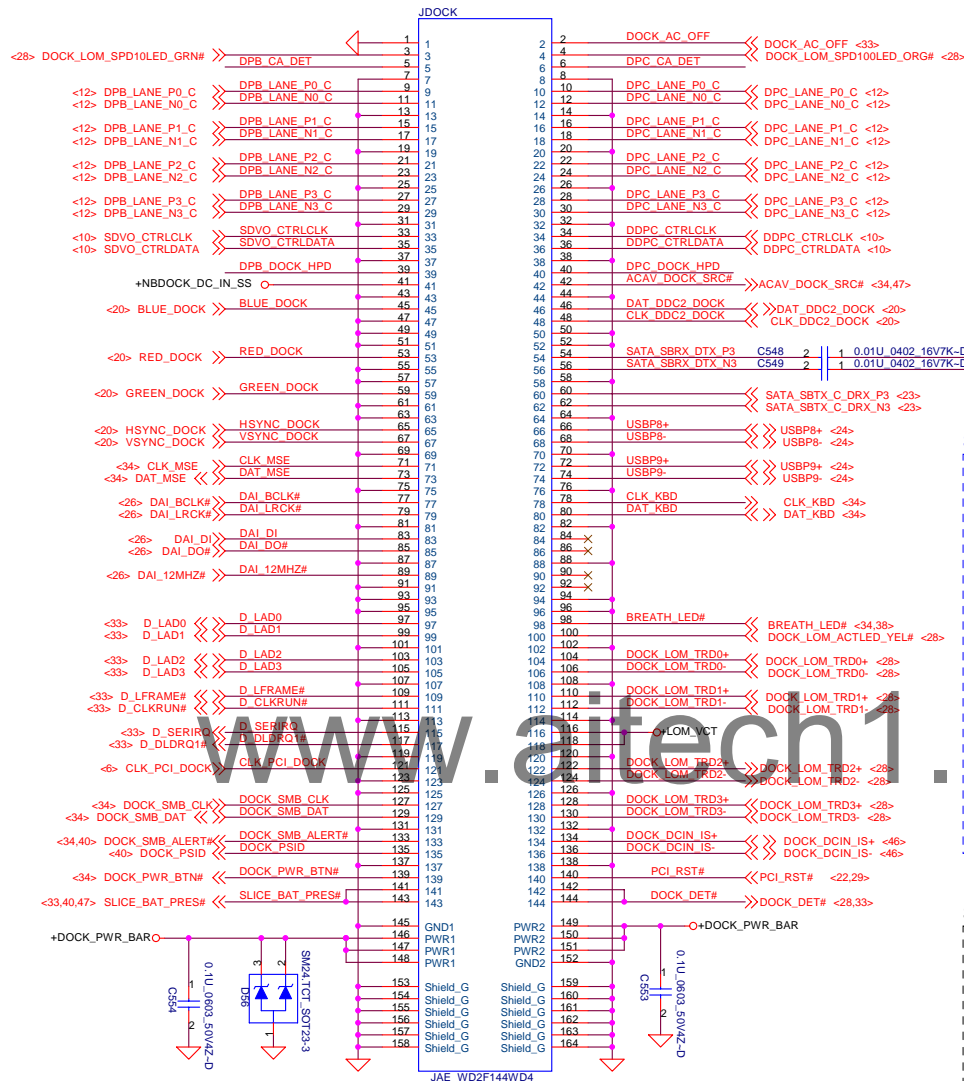
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Mini Card 2---WWAN



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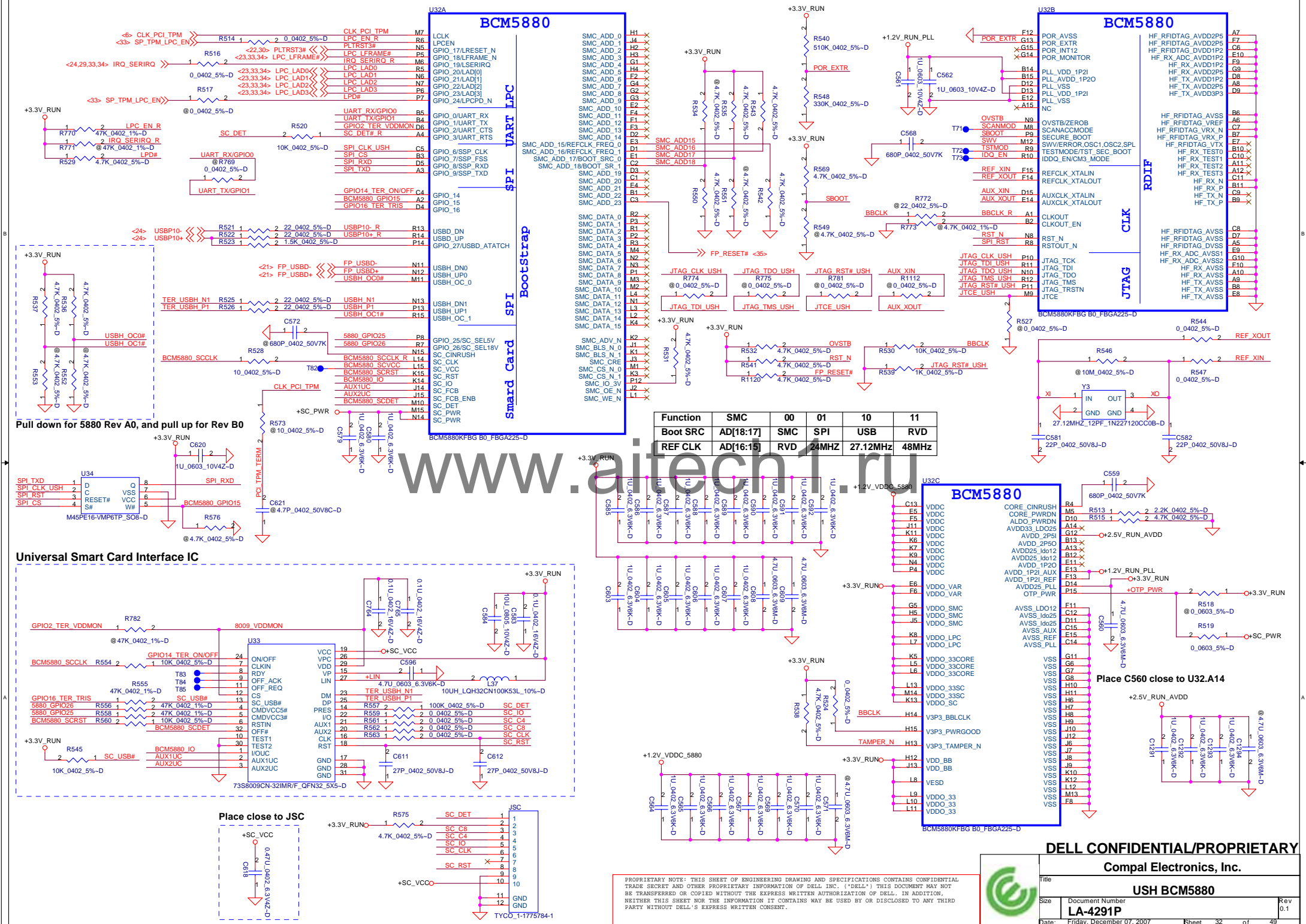
DPB_LANE_P0 C		1		10		DPB_LANE_P0 C	
DPB_LANE_N0 C	2			9		DPB_LANE_N0 C	
DPB_LANE_P1 C	4			7		DPB_LANE_P1 C	
DPB_LANE_N1 C	5			6		DPB_LANE_N1 C	
		3					
		8					
		RCLAMP0524P.TCT-D					
DPB_LANE_P2 C		1		10		DPB_LANE_P2 C	
DPB_LANE_N2 C	2			9		DPB_LANE_N2 C	
DPB_LANE_P3 C	4			7		DPB_LANE_P3 C	
DPB_LANE_N3 C	5			6		DPB_LANE_N3 C	
		3					
		8					
		RCLAMP0524P.TCT-D					
SDVO_CTRLCLK		1		10		SDVO_CTRLCLK	
SDVO_CTRLDATA	2			9		SDVO_CTRLDATA	
DPB_DOCK_HPD	4			7		DPB_DOCK_HPD	
DPB_CA_DET	5			6		DPB_CA_DET	
		3					
		8					
		RCLAMP0524P.TCT-D					
DPC_LANE_P0 C		1		10		DPC_LANE_P0 C	
DPC_LANE_N0 C	2			9		DPC_LANE_N0 C	
DPC_LANE_P1 C	4			7		DPC_LANE_P1 C	
DPC_LANE_N1 C	5			6		DPC_LANE_N1 C	
		3					
		8					
		RCLAMP0524P.TCT-D					
DPC_LANE_P2 C		1		10		DPC_LANE_P2 C	
DPC_LANE_N2 C	2			9		DPC_LANE_N2 C	
DPC_LANE_P3 C	4			7		DPC_LANE_P3 C	
DPC_LANE_N3 C	5			6		DPC_LANE_N3 C	
		3					
		8					
		RCLAMP0524P.TCT-D					
DDPC_CTRLCLK		1		10		DDPC_CTRLCLK	
DDPC_CTRLDATA	2			9		DDPC_CTRLDATA	
DPC_DOCK_HPD	4			7		DPC_DOCK_HPD	
DPC_CA_DET	5			6		DPC_CA_DET	
		3					
		8					
		RCLAMP0524P.TCT-D					



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Function	SMC	00	01	10	11
Boot SRC	AD[18:17]	SMC	SPI	USB	RVD
REF CLK	AD[16:15]	RVD	24MHz	27.12MHz	48MHz

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USH BCM5880

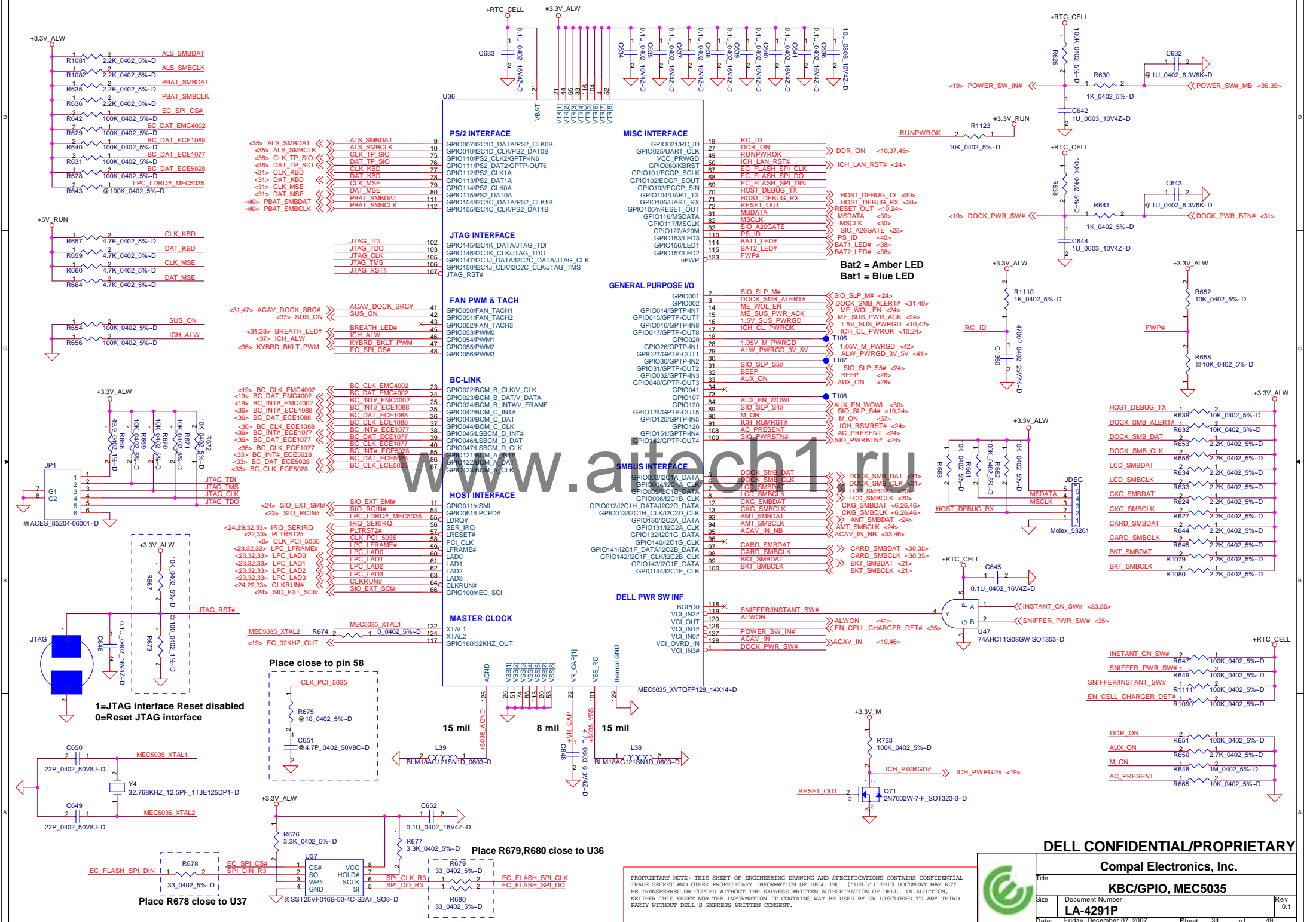
LA-4291P

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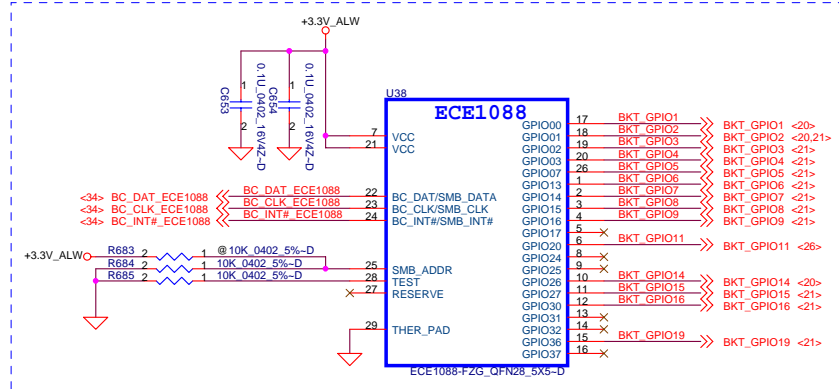


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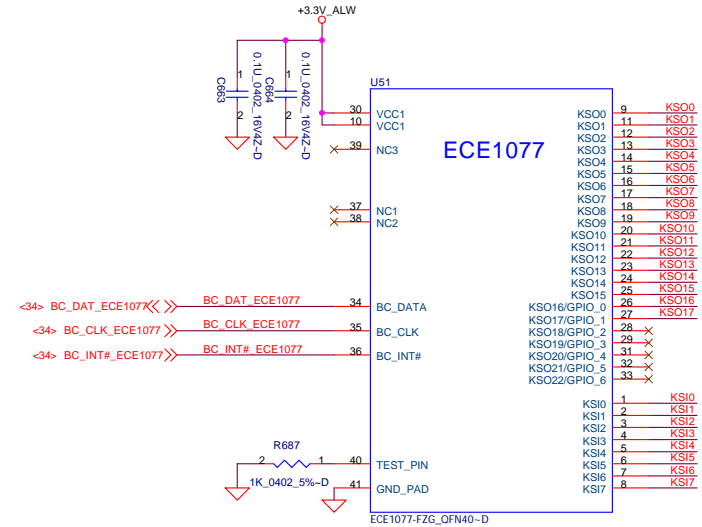
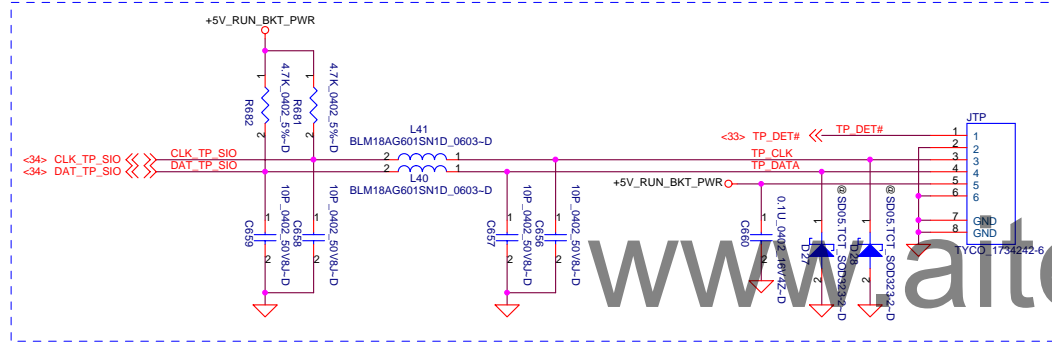
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KBC/GPIO, MEC5035	
Title	LA-4291P
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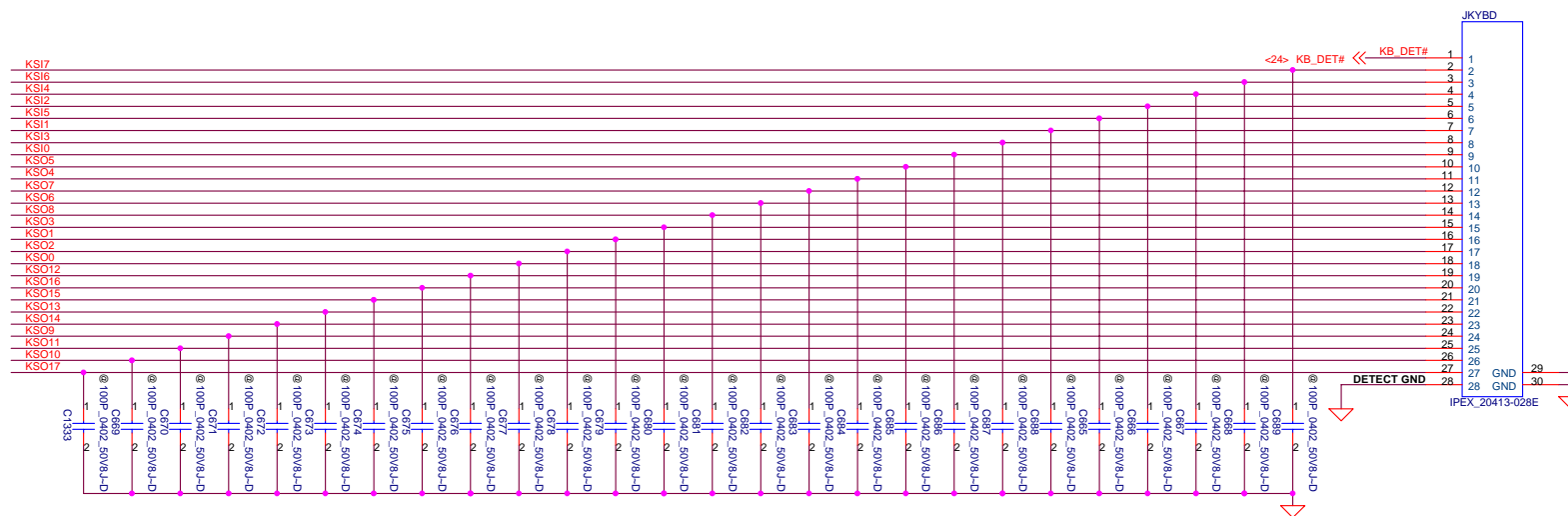
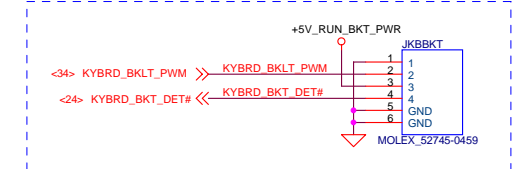
GPIO Expander for BlackTop



Touch Pad connector



Keyboard Backlight connector



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Title Keyboard, TouchPad and GPIO expander

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[illegible]

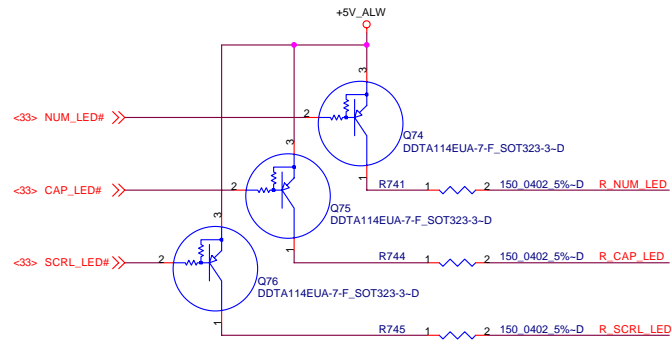
The left diagram shows the connection for the **SUS_ON** pin. It is connected to a **3.3V SUS** supply through a resistor **R718 @ 1K_0402_5%-D**. A Schottky diode **Q64 @ 2N7002W-7-F_SOT323-3-D** is connected in parallel with the pin to ground. The pin is labeled **SUS_ON 3.3V#** and has a pin number **2** and a ground symbol.

The right diagram shows the connection for the **RUN_ON_ENABLE** pin. It is connected to a **3.3V RUN** supply through a resistor **R716 @ 1K_0402_5%-D**. A Schottky diode **Q62 @ 2N7002W-7-F_SOT323-3-D** is connected in parallel with the pin to ground. The pin is labeled **RUN_ON_ENABLE#** and has a pin number **2** and a ground symbol.

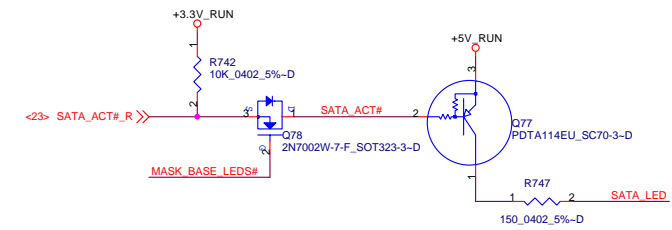


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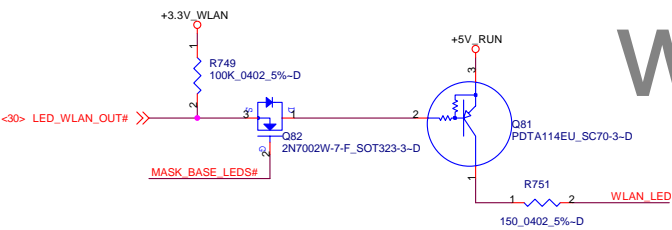
Keyboard Status, Num Lock/Caps Lock/Scroll Lock LEDs



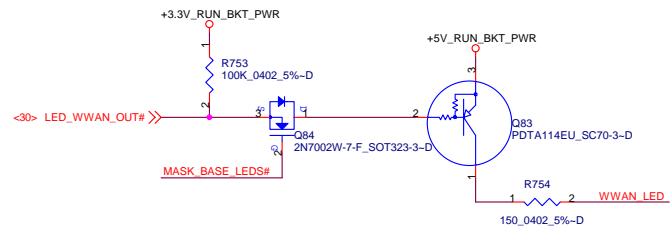
HDD LED



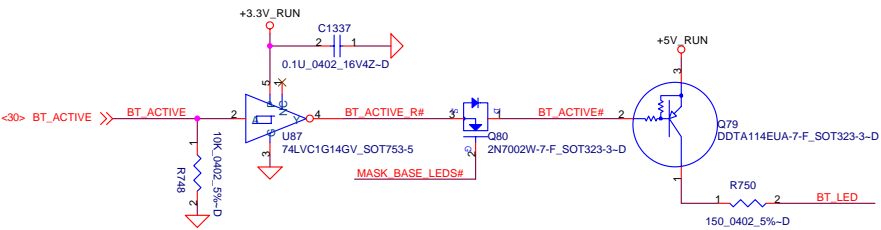
WLAN LED



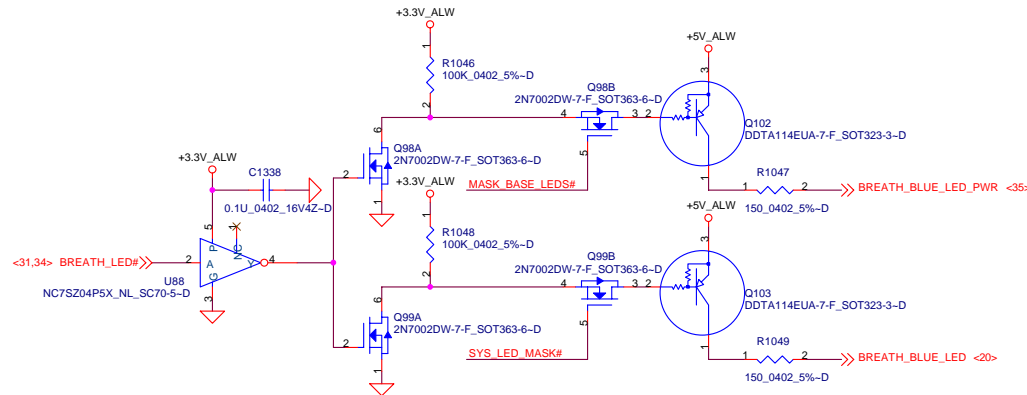
WWAN LED



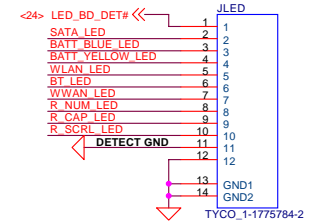
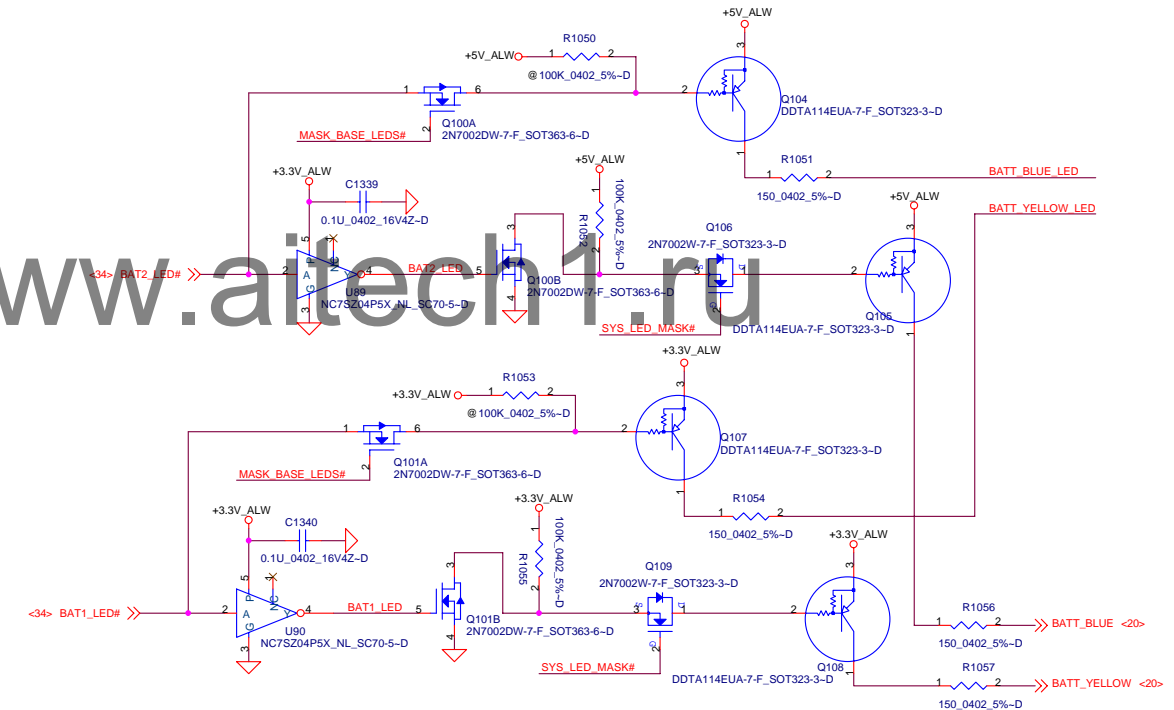
BLUETOOTH LED



POWER/SUSPEND breathing LED

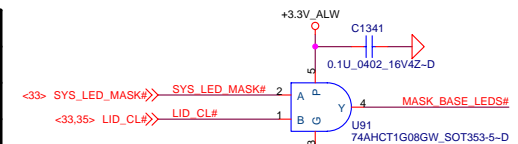


BATTERY LED



LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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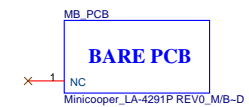
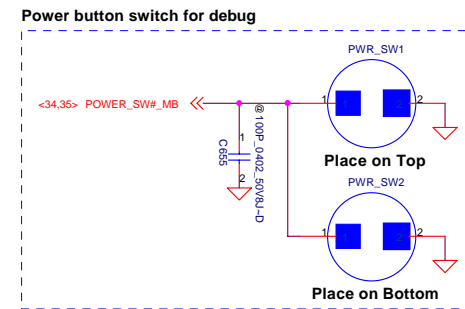
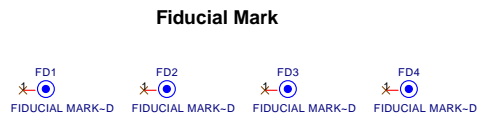
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System LEDs Control

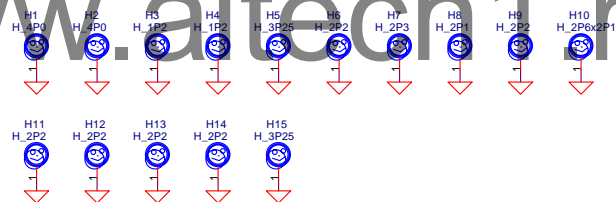
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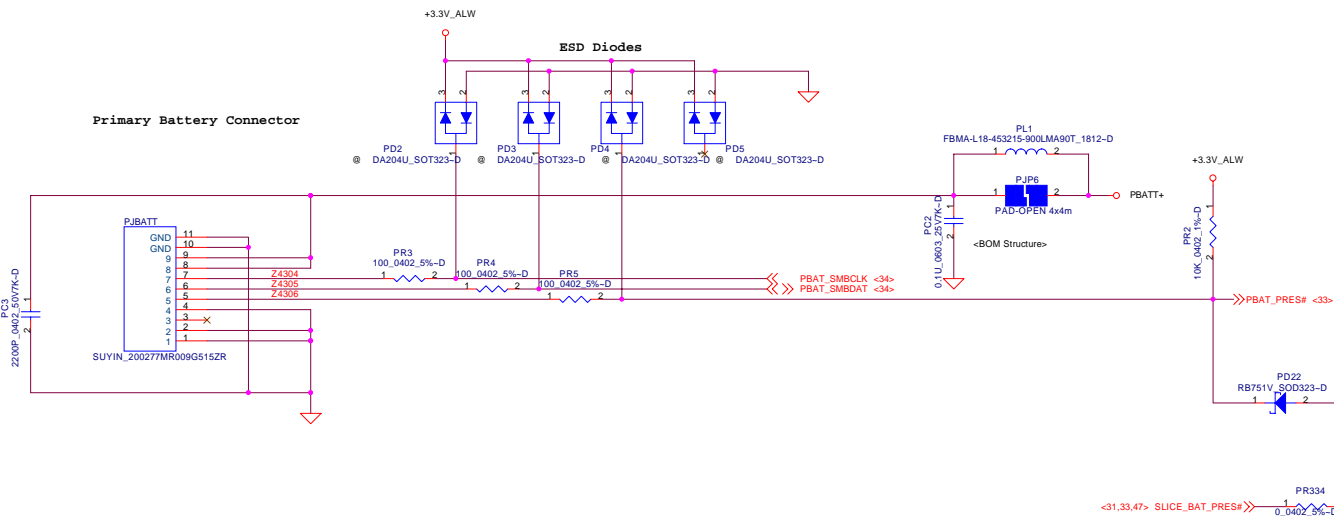


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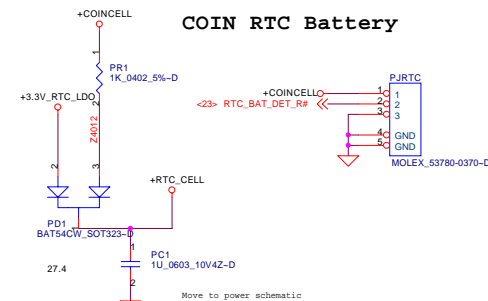


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Standoff and EE Design Part				
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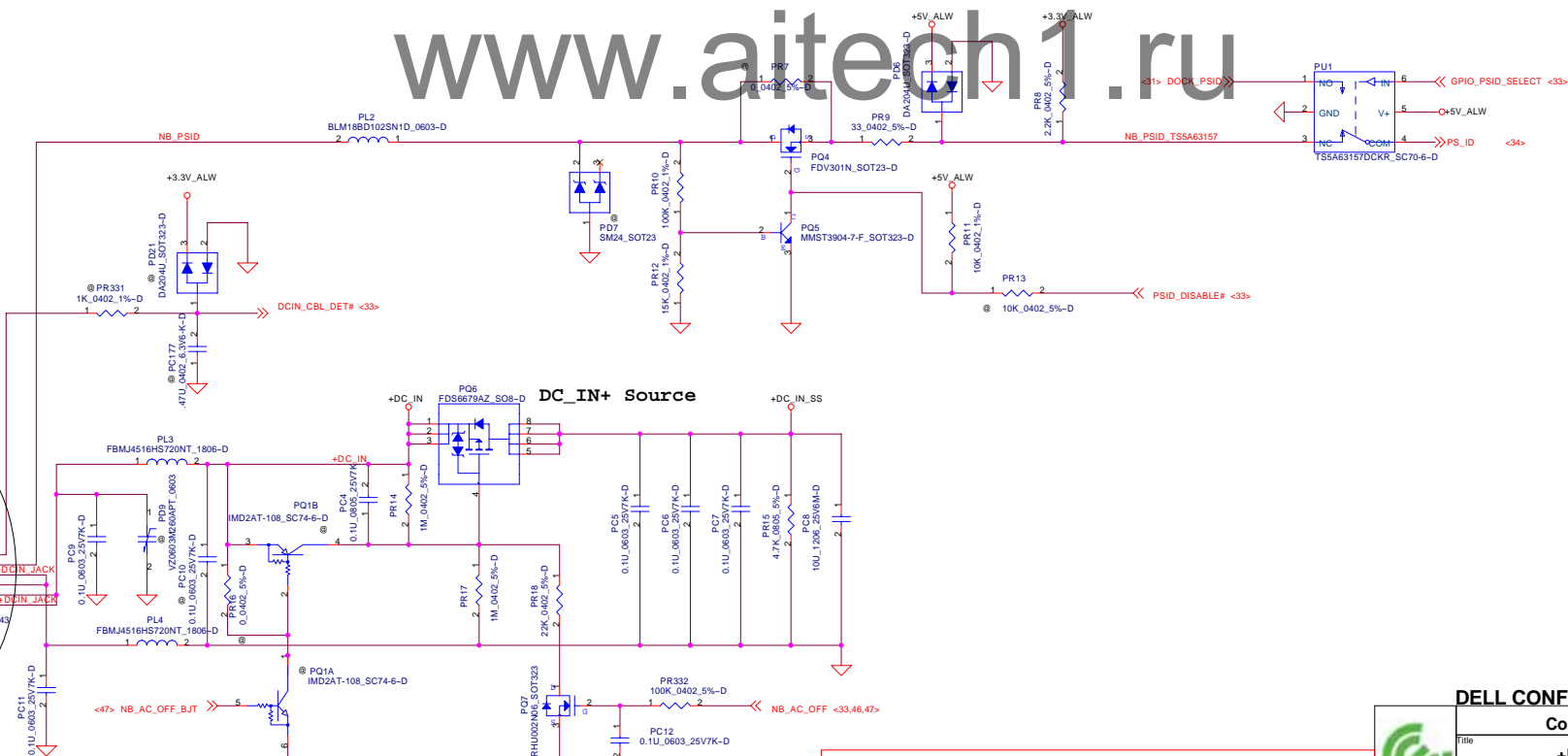
Primary Battery Connector



COIN RTC Battery



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+3.3V_ALWP/ +5V_ALWP/ +5V_ALW2 / +15V_ALWP

5 Volt +/-5%
Thermal Design Current:7.39A
Peak current: 10.55A
OCP min: 11A

3.3 Volt +/-5%
Thermal Design Current: 6.73A
Peak current: 9.62A
OCP min: 11A

VOUT1=5V
L=2.2uF
Fsw=400KHz
D=0.256
Output Ripple Current=4.23A
Output Ripple Voltage=4.23A*18mOhm=76.14mV

VOUT2=3.3V
L=2.2uF
Fsw=500KHz
D=0.169
Output Ripple Current=2.49A
Output Ripple Voltage=2.49A*25mOhm=62.25mV

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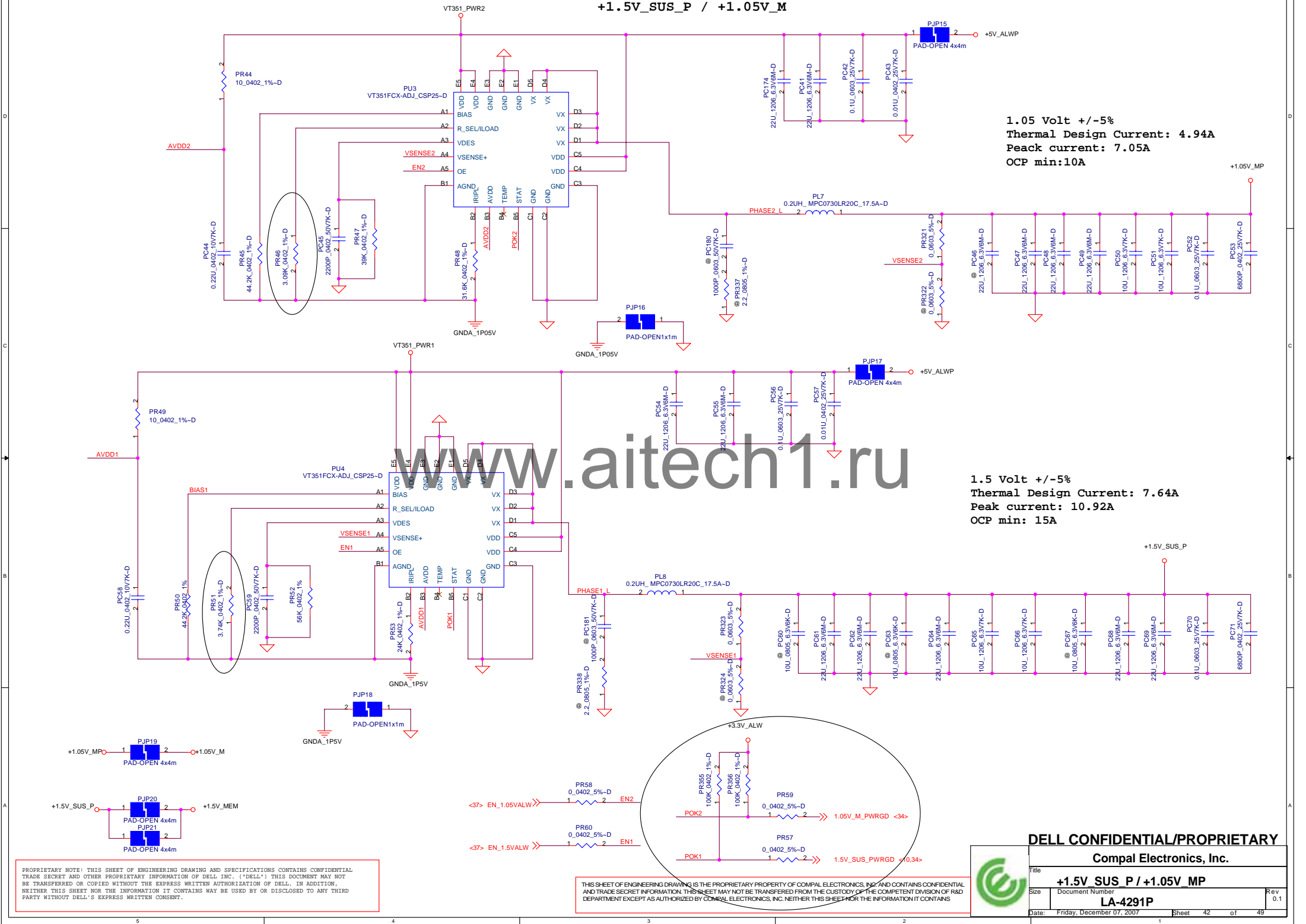
DC/DC +3V/ +5V

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+1.5V_SUS_P / +1.05V_M




1.05 Volt +/-5%
Thermal Design Current: 4.94A
Peak current: 7.05A
OCP min:10A

1.5 Volt +/-5%
Thermal Design Current: 7.64A
Peak current: 10.92A
OCP min: 15A

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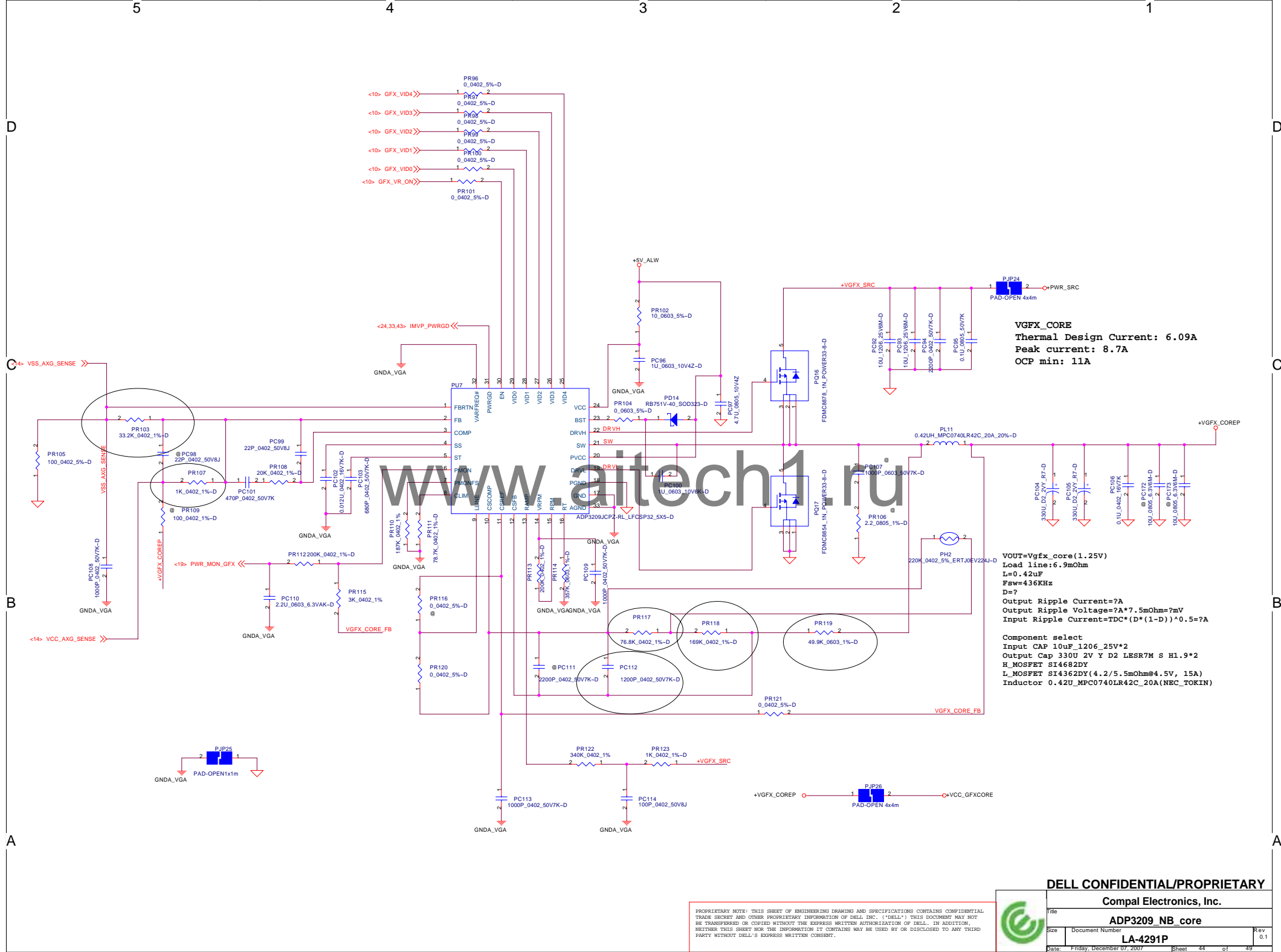
+1.5V_SUS_P / +1.05V_MP

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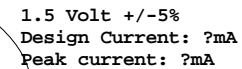
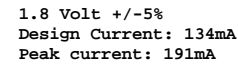
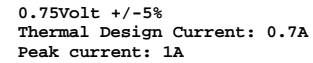


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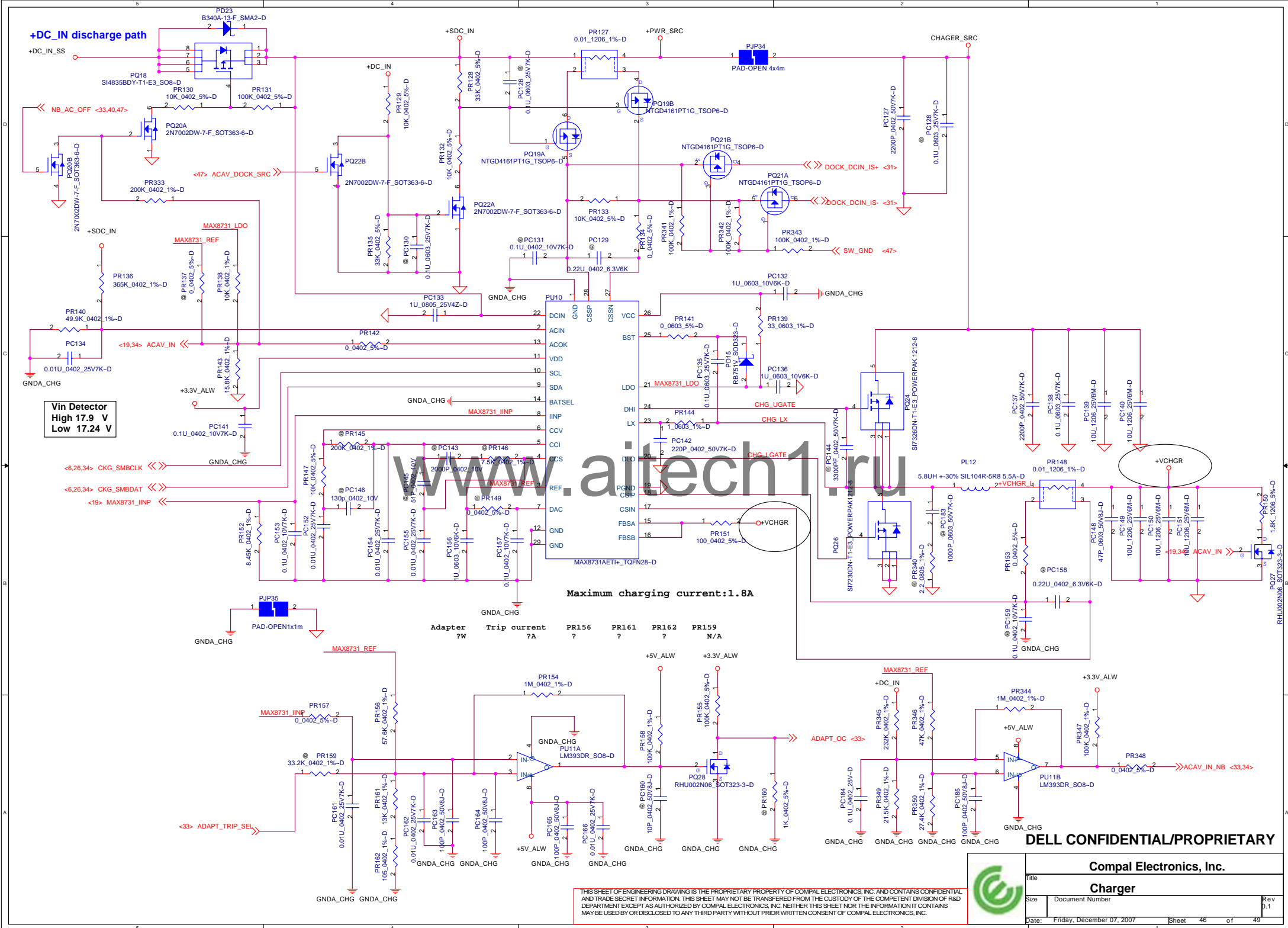


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DDR3 Termination



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